NV156FHM-T01 V8.0

Product Specification

Rev. 0

BOE Optoelectronics Technology Co., Ltd

REVISION HISTORY

Revision No.	Page	Description of Changes	Date	Prepared
0	34	Final Release	2018.05.23	Liu Huaqing

REVIEWED	
Designer	**Manager**
Zhou Houfeng(Array)	Huang Zhonghao
Pan Ruiqi (Cell)	Hu Jingyong
Sun Yulong(CF)	Li Min
Qin Peng(EE)	Zuo Cheng
Liu Song(MO)	Gao Liang
Long Yi(QE)	Huang Yuan
Tang Taoliang(PI)	Tang Xiuzhu
APPROVED	
Zhu Wei(PM)	

Contents

1.0 GENERAL DESCRIPTION

1.1 Introduction

NV156FHM-T01 V8.0 is a color active matrix TFT LCD module using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 15.6 inch diagonally measured active area with Full-HD resolutions (1920 horizontal by 1080 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 262k(6bit) colors and color gamut 45%. The TFT-LCD panel used for this module is a low reflection and higher color type. Therefore, this module is suitable for Notebook PC. The LED driver for back-light driving is built in this model.
All input signals are eDP1.2 interface compatible.

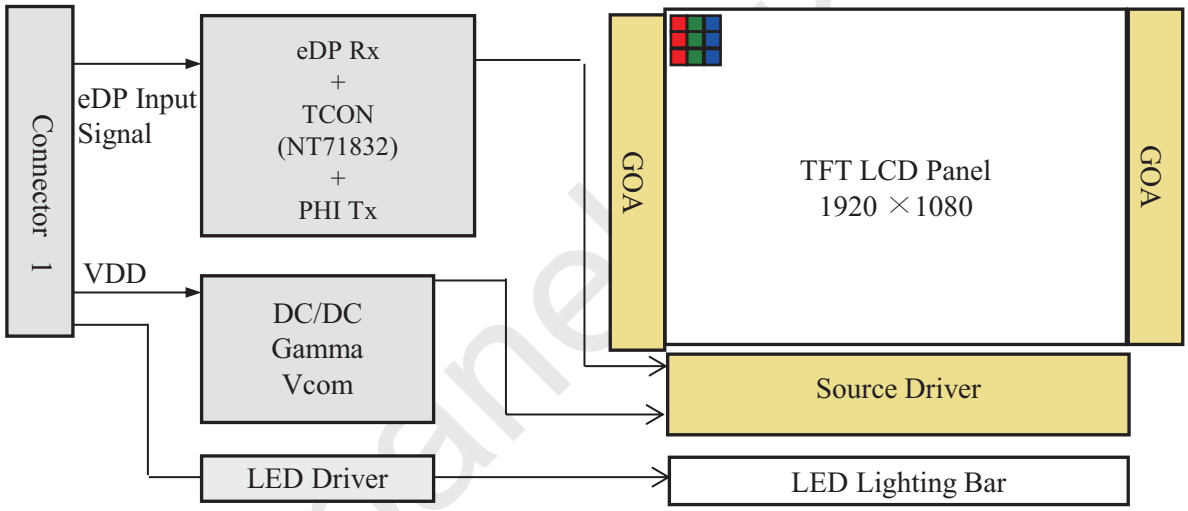


Figure 1. Drive Architecture

1.2 Features

- 2 lane eDP interface with 2.7Gbps link rates
- Thin and light weight
- 262k(6bit) color depth, color gamut 45%
- Single LED lighting bar (Bottom side/Horizontal Direction)
- Data enable signal mode
- Side mounting frame
- Green product (RoHS & Halogen free product)
- On board LED driving circuit
- Low driving voltage and low power consumption
- On board EDID chip

1.3 Application

● Notebook PC (Wide type)

1.4 General Specification

The followings are general specifications at the model NV156FHM-T01 V8.0. (listed in Table 1)

<Table 1. General Specifications>

Parameter	Specification	Unit	Remarks
Active area	344.16(H) ×193.59(V)	mm	
Number of pixels	1920 (H) ×1080 (V)	pixels	
Pixel pitch	179.25(H) ×179.25(V)	um	
Pixel arrangement	RGB Vertical stripe		
Display colors	262k(6bit)		
Color gamut	45%		
Display mode	Normally Black		
Dimensional outline	350.66(H) ×216.15(V) (W/PCB) ×3.2max(panel side) 3.4max(PCBA side)	mm	
Weight	385 (max)	g	
Surface treatment	Glare		
Surface hardness	3H		
Back-light	Bottom edge side, 1-LED lighting bar type		Note 1
Power consumption	P_D : 0.9	W	@Mosaic
	P_{BL} : 3.6	W	
	P_{Total} : 4.5	W	@Mosaic

Notes : 1. LED Lighting Bar (40*LED Array

1.5 General Touch Specification(Table 2.)

<Table 2. General Touch Specifications>

Parameter	Specification	Unit	Remarks
Type of Touch Sensor	Self Capacitance		
Touch Structure	On Cell		
Panel Size	15.6”		
Outline Dimension	350.66(H) ×216.15(V) (W/PCB) ×3.2max(panel side) 3.4max(PCBA side)	mm	
TP View Area	N/A(Cover Lens Free)	mm	
TP Active Area	X 344.16 × Y 193.59（AA）	mm	
Total Thickness	N/A(Cover Lens Free)	mm	
Interface	USB		
Report Rate	Follow win10 – 100Hz		
Multi-Touch Point	10 points		
Input method	Finger		
Touch panel sensor IC	G7500		
Channel	1500		
Surface treatment	Glare		
Surface Hardness	3	H	
Support OS	Win8.x and Win10 compliant		
TP Power Consumption	200 max.	mW	@ 5 finger

2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 3.

< Table 3. Absolute Maximum Ratings>

Ta=25+/-2˚C

Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-0.3	4.0	V	Note 1
Logic Supply Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V	
Operating Temperature	T_{OP}	0	+50	˚C	Note 2
Storage Temperature	T_{ST}	-20	+60	˚C	

Notes :
1. Permanent damage to the device may occur if maximum values are exceeded functional operation should be restricted to the condition described under normal operating conditions.
2. Temperature and relative humidity range are shown in the figure below.
95 % RH Max. (40 ˚C ≥ Ta) Maximum wet - bulb temperature at 39 ˚C or less. (Ta > 40 ˚C) No condensation.

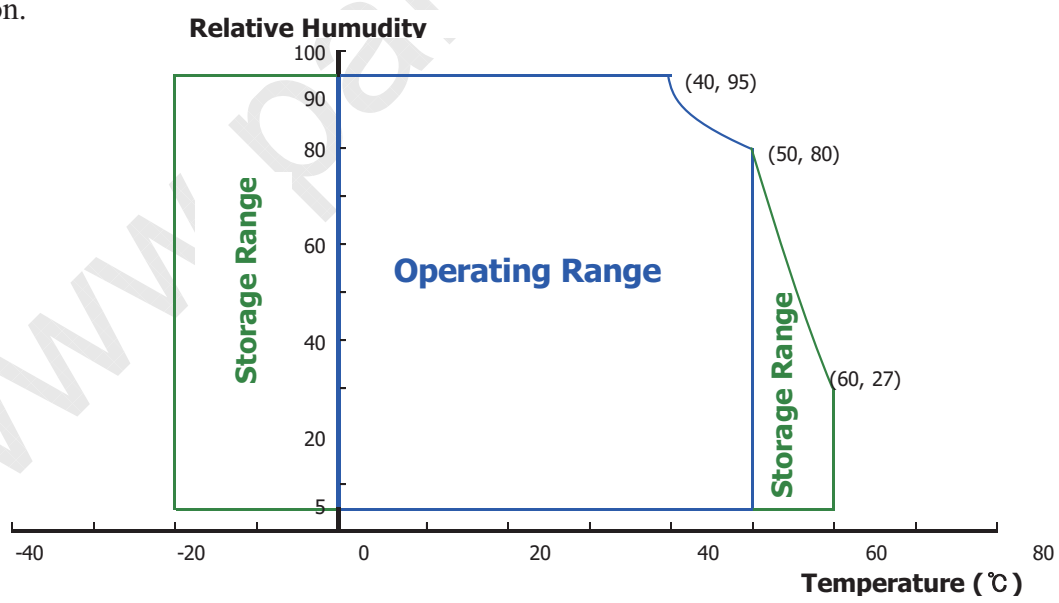


Figure 2. Temperature and Relative Humidity Range

3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Specifications

< Table 4. Electrical Specifications > Ta=25+/-2°C

Parameter		Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	3.0	3.3	3.6	V	Note 1
Permissible Input Ripple Voltage	V_{RF}	-	-	100	mV	@ V_{DD} = 3.3V
BIST Control Level	High Level	2	-	3.6	V	-
	Low Level	0	-	0.8	V	-
Power Supply Current	I_{DD}	-	273	583	mA	Note 1
Power Supply Inrush Current	Inrush	-	-	1.5	A	Note3
Power Consumption	P_D	-	0.9	1.60	W	Note 1
	P_{BL}	-	-	3.6	W	Note 2
	P_{total}	-	-	5.2	W	

Notes :

1. The supply voltage is measured and specified at the interface connector of LCM.
   The current draw and power consumption specified is for 3.3V at 25 °C.
   a) Typ : Mosaic pattern 8*8
   b) Max : R/G/B patterns

(a) (b)

Figure 3. Power Measure Patterns

2. Calculated value for reference (V_{LED} × I_{LED})
3. Measure condition (Figure 4)

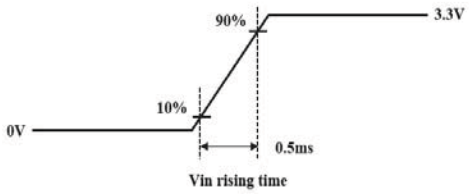


Figure 4. Inrush Measure Condition

3.2 Backlight Unit

< Table 5. LED Driving Guideline Specifications > Ta=25+/-2°C

Parameter			Min.	Typ.	Max.	Unit	Remarks
LED Forward Voltage		V_F	-	-	3.0	V	-
LED Forward Current		I_F	-	23.4	-	mA	-
LED Power Consumption		P_{LED}	-	-	3.6	W	Note 1
LED Life-Time		N/A	15,000	-	-	Hour	I_F = 23.4mA
Power Supply Voltage for LED Driver		V_{LED}	5	12	21	V	-
Power Supply Voltage for LED Driver Inrush		Iled inrush	-	-	1.5	A	Note 4
EN Control Level	Backlight On		2.5	-	5.0	V	-
	Backlight Off		0	-	1.0	V	-
PWM Control Level	High Level		2.5	-	5.0	V	-
	Low Level		0	-	1.0	V	-
PWM Control Frequency		F_{PWM}	200	-	10,000	Hz	-
Duty Ratio			1	-	100	%	Note 3

Notes :
1. Power supply voltage12V for LED driver.
   Calculator value for reference IF × VF ×40 /driver efficiency = PLED
2. The LED life-time define as the estimated time to 50% degradation of initial luminous.
3. 1% duty cycle is achievable with a dimming frequency less than 1KHz.
4. Measure condition (Figure 5)

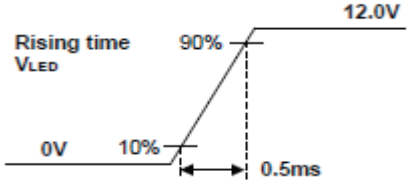


Figure 5. Inrush Measure Condition

3.3 LED Structure

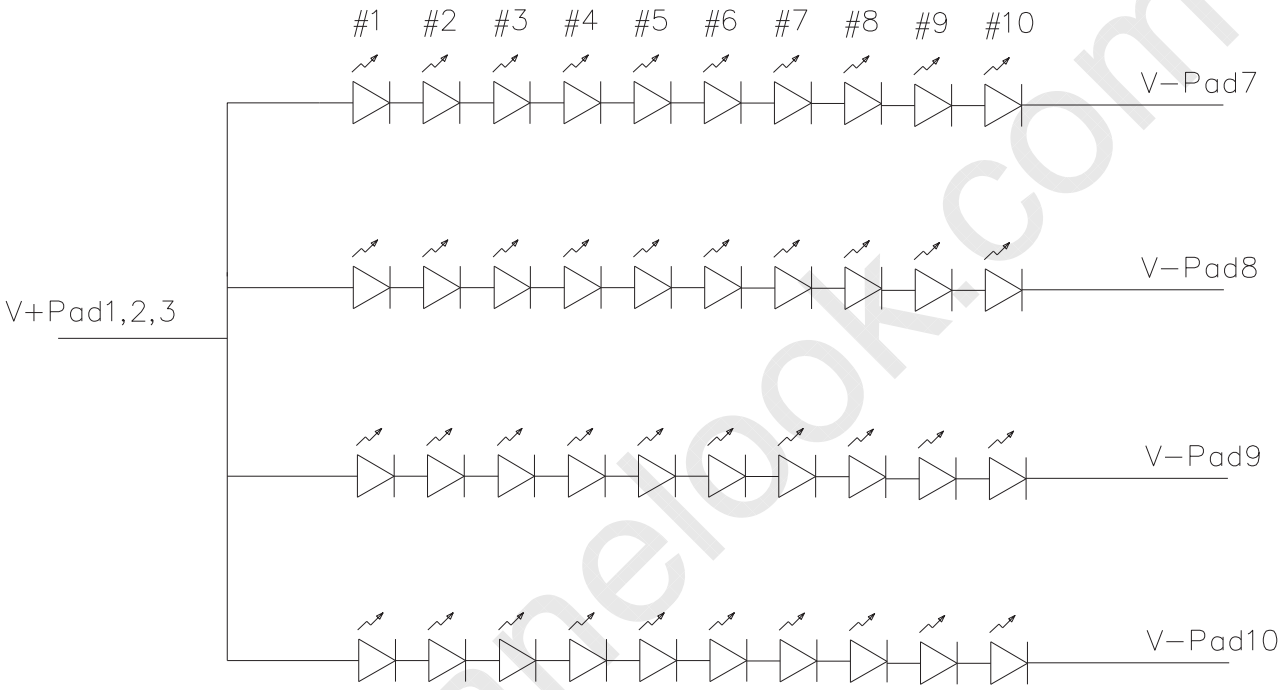


Figure 6. LED Structure

4.0 OPTICAL SPECIFICATION

4.1 Overview

The test of optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = 25±2℃) with the equipment of luminance meter system (PR730&PR810) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to θØ=0 (=θ3) as the 3 o'clock direction (the "right"), θØ=90 (= θ12) as the 12 o'clock direction ("upward"), θØ=180 (= θ9) as the 9 o'clock direction ("left") and θØ=270(= θ6) as the 6 o'clock direction ("bottom"). While scanning θand/or Ø, the center of the measuring spot on the display surface shall stay fixed. The backlight should be operating for 30 minutes prior to measurement. VDD shall be 3.3+/- 0.3V at 25°C. Optimum viewing angle direction is 6 'clock.

4.2 Optical Specifications

<Table 6. Optical Specifications>

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle Range	Horizontal	Θ_3	CR > 10	-	85	-	Deg.	Note 1
		Θ_9		-	85	-	Deg.	
	Vertical	Θ_{12}		-	85	-	Deg.	
		Θ_6		-	85	-	Deg.	
Luminance Contrast Ratio		CR	Θ = 0°	600	800	-		Note 2
Luminance of White	5 Points	Y_w	Θ = 0° ILED = 23.4mA	212.5	250	-	cd/m²	Note 3
White Luminance Uniformity	5 Points	ΔY5		80	-	-	%	Note 4
	13 Points	ΔY13		62.5	-	-	%	
White Chromaticity		W_x	Θ = 0°	0.283	0.313	0.343	-	Note 5
		W_y		0.299	0.329	0.359	-	
Reproduction of Color	Red	R_x	Θ = 0°	-0.03	0.590	+0.03	-	-
		R_y			0.350		-	-
	Green	G_x			0.330		-	-
		G_y			0.555		-	-
	Blue	B_x			0.153		-	-
		B_y			0.119		-	-
Color Gamut		-	-	-	45	-	%	-
Response Time (Rising + Falling)		T_{RT}	Ta= 25℃ Θ = 0°	-	30	35	ms	Note 6
Cross Talk		CT	Θ = 0°	-	-	2.0	%	Note 7

Notes :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 7).

2. Contrast measurements shall be made at viewing angle of Θ= 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see Figure 7) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Center Luminance of white is defined as luminance values of 5 point average across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 8 for a total of the measurements per display.

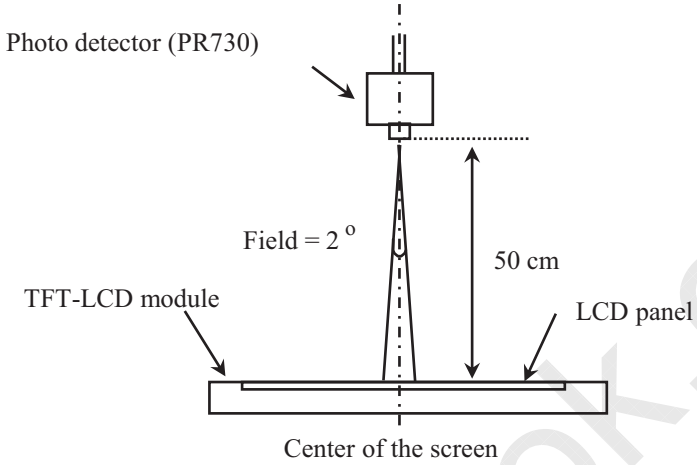
4. The White luminance uniformity on LCD surface is then expressed as : ΔY =Minimum Luminance of 5(or 13) points / Maximum Luminance of 5(or 13) points.(see Figure 8 and Figure 9).

5. The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

6. The electro-optical response time measurements shall be made as Figure 10 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is T_r, and 90% to 10% is T_f.

7.Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 10±1mm diameter area, with all display pixels set to gray 127(of 0 to 255), to the luminance (YB) of that same area when any adjacent area is driven dark.The luminance ratio shall not exceed 1:1.05 (See Figure 11).

4.3 Optical Measurements



Optical characteristics measurement setup

Figure 7. Measurement Set Up

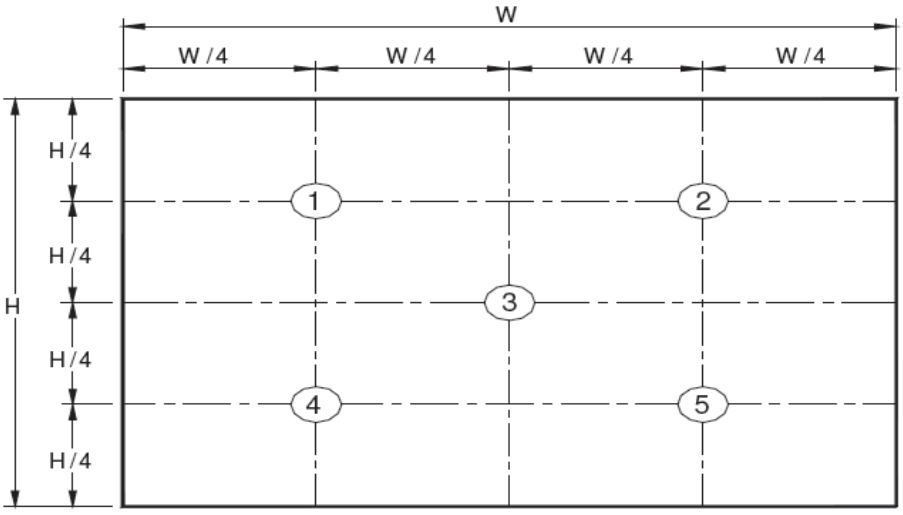


Figure 8. White Luminance and Uniformity Measurement Locations (5 points)

Center Luminance of white is defined as luminance values of center 5 points across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 7 for a total of the measurements per display.

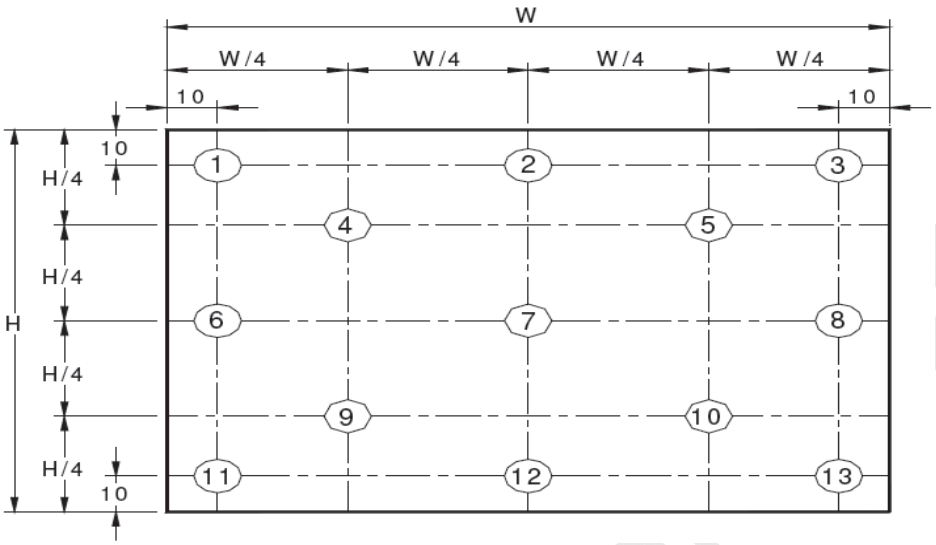


Figure 9. Uniformity Measurement Locations (13 points)

The White luminance uniformity on LCD surface is then expressed as : ΔY5 = Minimum Luminance of five points / Maximum Luminance of five points (see Figure 8) , ΔY13 = Minimum Luminance of 13 points /Maximum Luminance of 13 points (see Figure 9).

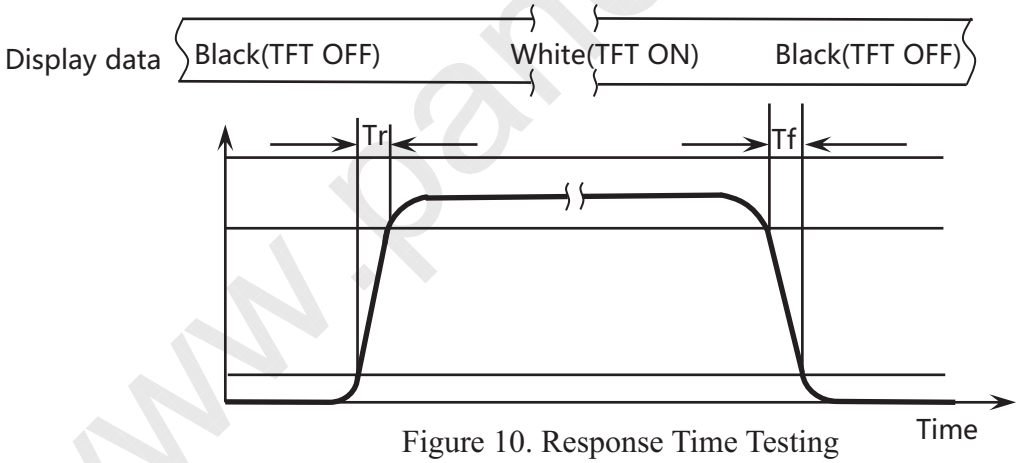
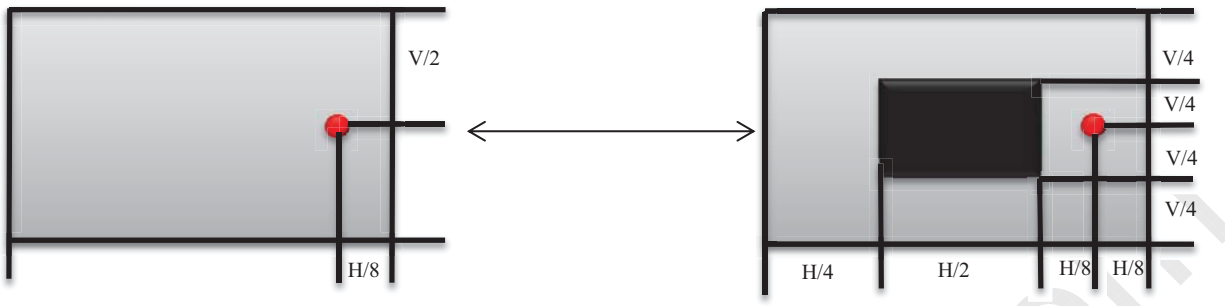


Figure 10. Response Time Testing

The electro-optical response time measurements shall be made as shown in Figure 10 by switching the "data" input signal ON and OFF. Tf: The luminance to change from 90% to 10% ,Tr: The luminance to change from 10% to 90% .

The test system : PR810



$$\text{Cross Talk (\%)} = \left| \frac{Y_B - Y_A}{Y_A} \right| \times 100$$

Figure 11. Cross Talk Modulation Test Description

Where:

Y_A = Initial luminance of measured area (cd/m^2)

Y_B = Subsequent luminance of measured area (cd/m^2)

The location 1/2/3/4 measured will be exactly the same in both patterns. The test background gray is from L64 to L192.Take the largest data as the result.

Cross Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (YB) of that same area when any adjacent area is driven dark.(Refer to Figure 11)

The test system: PR730

5.0 INTERFACE CONNECTION

5.1 Electrical Interface Connection

The electronics interface connector is 20455-040E-66.
The connector interface pin assignments are listed in Table 7.

<Table 7. Pin Assignments for the Interface Connector>

Terminal	Symbol	Functions
Pin No.	Symbol	Description
1	NC	No Connect (Reserved for DCR)
2	H_GND	High Speed Ground
3	Lane1_N	Comp Signal Link Lane 1
4	Lane1_P	True Signal Link Lane 1
5	H_GND	High Speed Ground
6	Lane0_N	Comp Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Comp Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	LCD_Self_Test or NC	LCD Panel Self Test Enable (Optional)
15	LCD_GND	LCD logic and driver ground
16	LCD_GND	LCD logic and driver ground
17	HPD	HPD signal pin
18	BL_GND	Backlight ground
19	BL_GND	Backlight ground
20	BL_GND	Backlight ground
21	BL_GND	Backlight ground
22	BL_Enable	Backlight On / Off
23	BL_PWM_DIM	System PWM signal Input
24	NC	No connect (Reverse for TEST only)
25	NC	No connect (Reverse for TEST only)
26	BL_PWR	Backlight power (5V~21V)
27	BL_PWR	Backlight power (5V~21V)
28	BL_PWR	Backlight power (5V~21V)
29	BL_PWR	Backlight power (5V~21V)
30	NC	No Connect (Reserved for CM)

5.0 INTERFACE CONNECTION

5.1 Electrical Interface Connection

The electronics interface connector is 20455-040E-66.
The connector interface pin assignments are listed in Table 7.

<Table 7. Pin Assignments for the Interface Connector>

Terminal	Symbol	Functions
Pin No.	Symbol	Description
31	TP_D-	USB Data- for Touch
32	TP_D+	USB Data+ for Touch
33	GND	Ground–Shield
34	VTSP	Touch panel power supply (3.3V)
35	VTSP	Touch panel power supply (3.3V)
36	NC/TP_EN	Reserve for Touch function enable (Low_Disable & High_Enable)
37	TP_CLK	I2C Clock for Touch (NC for USB input)
38	TP_Data	I2C Data for Touch (NC for USB input)
39	INT	Interrupt for Touch (NC for USB input)
40	RST	Reset for Touch (NC for USB input)

5.2 eDP Interface

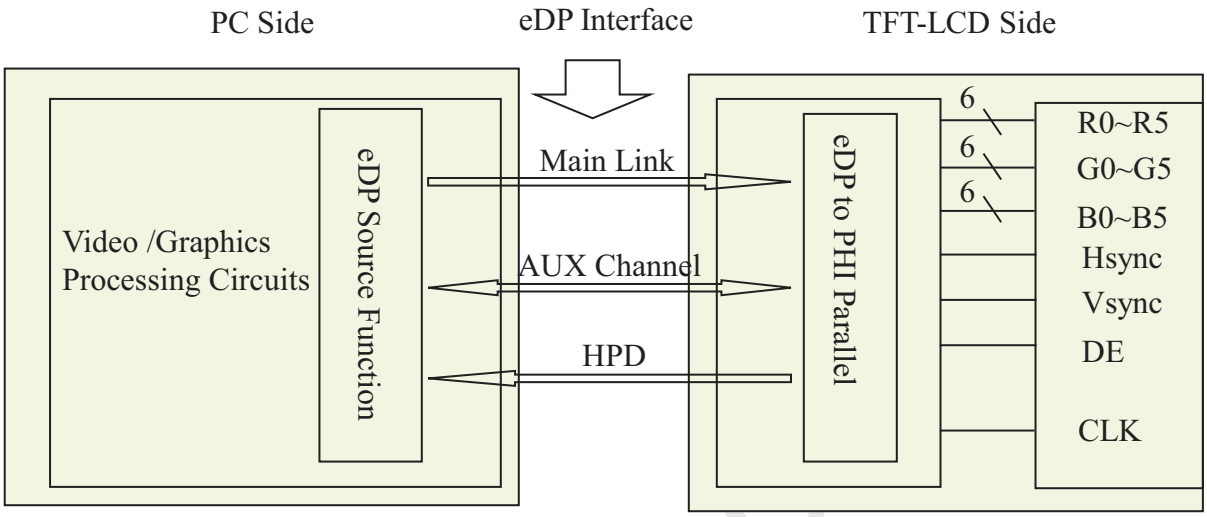


Figure 12. eDP Interface Architecture

Note:
Transmitter : NT71832 or equivalent.
Transmitter is not contained in module.

5.3 Data Input Format

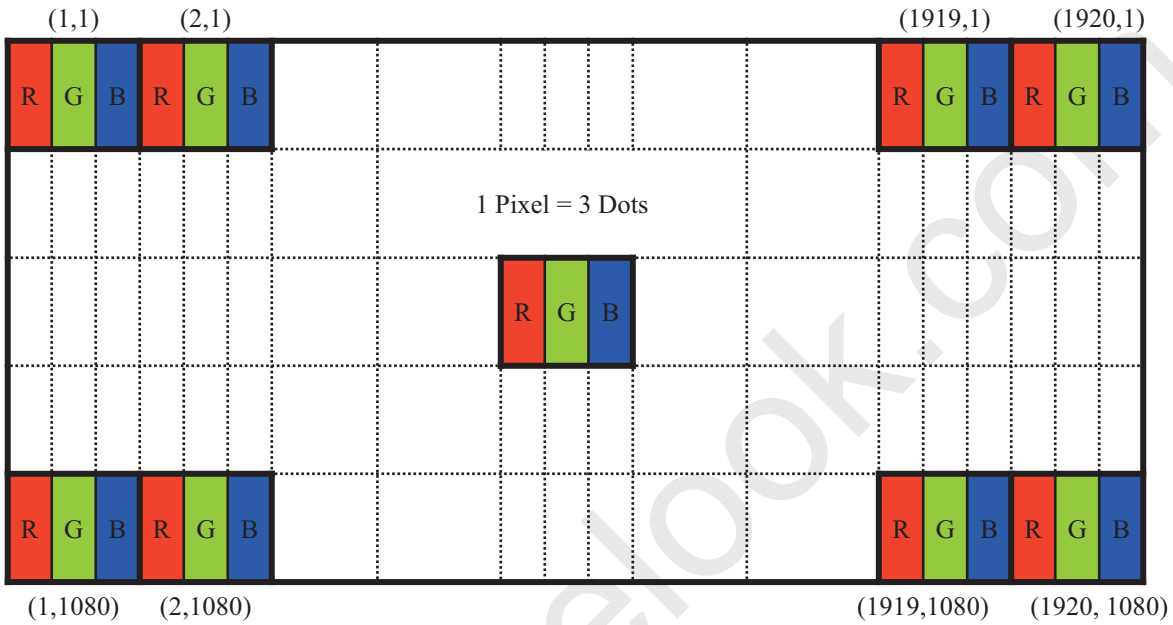


Figure 13. Display Position of Input Data (V-H)

5.4 Back-light & LCM Interface Connection

BLU Interface Connector: STM MSK24022P10.

<Table 8. Pin Assignments for the BLU Connector>

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	Vout	LED anode connection	6	NC	NC Connection
2	Vout	LED anode connection	7	LED1	LED cathode connection
3	Vout	LED anode connection	8	LED2	LED cathode connection
4	NC	NC	9	LED3	LED cathode connection
5	NC	NC	10	LED4	LED cathode connection

6.0 SIGNAL TIMING SPECIFICATION

6.1 The NV156FHM-T01 V8.0 Is Operated By The DE Only

< Table 9. Signal Timing Specification >

Item		Symbols	Min	Typ	Max	Unit
Clock	Frequency	1/Tc	137.1	141.4	146.6	MHz
Frame Period		Tv	1098	1100	1130	lines
			-	60	-	Hz
			-	16.67	-	ms
Vertical Display Period		Tvd	-	1080	-	lines
One line Scanning Period		Th	2080	2142	2153	clocks
Horizontal Display Period		Thd	-	1920	-	clocks

Note : The above is as optimized setting.

6.2 eDP Rx Interface Timing Parameter

The specification of the eDP Rx interface timing parameter is shown in Table 10.

<Table 10. eDP Main-Link RX TP4 Package Pin Parameters>

Item	Symbol	Min	Typ	Max	Unit	Remark
Spread spectrum clock (Link clock down-spreading)	ssc	-	-	0.5	%	
Differential peak-to-peak input voltage at package pins	VRX-DIFFp-p	120	-	1200	mV	
Rx input DC common mode voltage	VRX_DC_CM	0	-	2	V	
Differential termination resistance	RRX-DIFF	80	100	120	Ω	
Single-ended termination resistance	RRX-SE	40	-	60	Ω	
Rx short circuit current limit	IRX_SHORT	-	-	50	mA	
Intra-pair skew at Rx package pins (HBR) RX intra-pair skew tolerance at HBR	LRX_SKEW_ INTRA_PAIR	-	-	60	ps	

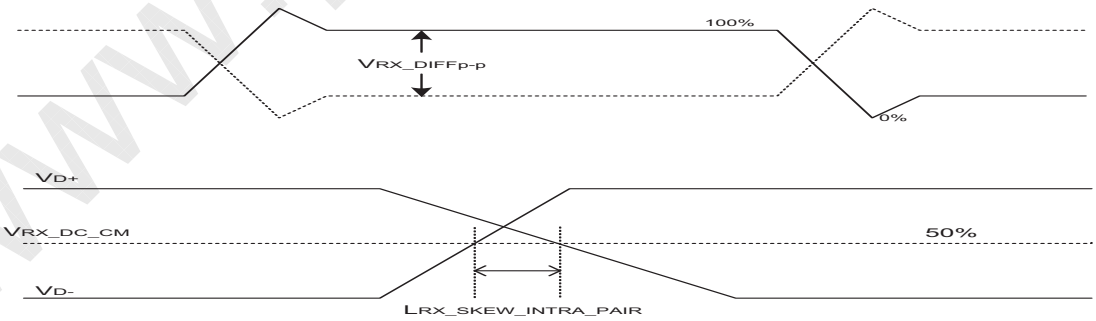
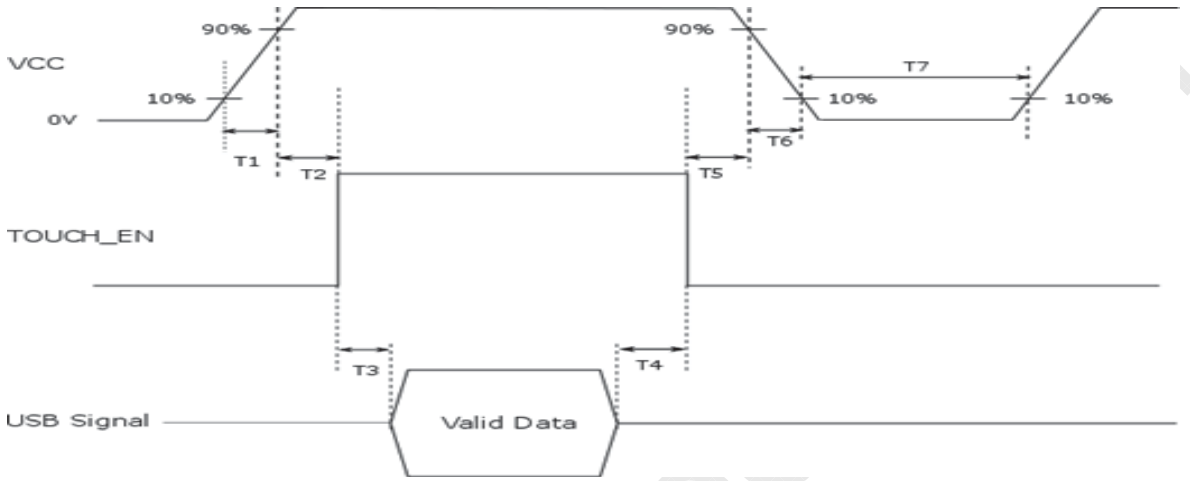


Figure 14. VRX-DIFFp-p & LRX_SKEW_INTRA_PAIR

6.3 Touch Interface Timing Parameter

The specification of the Touch interface timing parameter is shown in Table 10.2

<Table 10.2 Touch Interface Timing Specification>



Time	Min.	Typ.	Max.	Unit
T1	0	-	∞	ms
T2	-	-	10	ms
T2+T3	200	-	-	ms
T4+T5	5	-	-	ms
T5	-	-	0	ms
T6	33	-	∞	us
T7	10	-	∞	us

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Supply Voltage	VTSP	-	3.3	-	V	
USB Signal	TP_D+, TP_D-	-	3.3	-	V	
TP_Enable	TP_EN	-	3.3	-	V	

7.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

<Table 11. Input Signal & Basic Display Colors & Gray Scale of Colors >

	Colors & Gray scale	Data signal																	
		R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	B4	B5
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Light Blue	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Purple	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△ ▽			↑ ↓						↑ ↓						↑ ↓			
	Brighter	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	▽	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	△ ▽			↑ ↓						↑ ↓						↑ ↓			
	Brighter	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0
	▽	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
	△ ▽			↑ ↓						↓ ↓						↑ ↓			
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1
	▽	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
Gray scale of White & Black	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0
	Darker	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0
	△ ▽			↑ ↓						↑ ↓						↑ ↓			
	Brighter	1	0	1	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1
	▽	0	1	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1	1
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

8.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below.

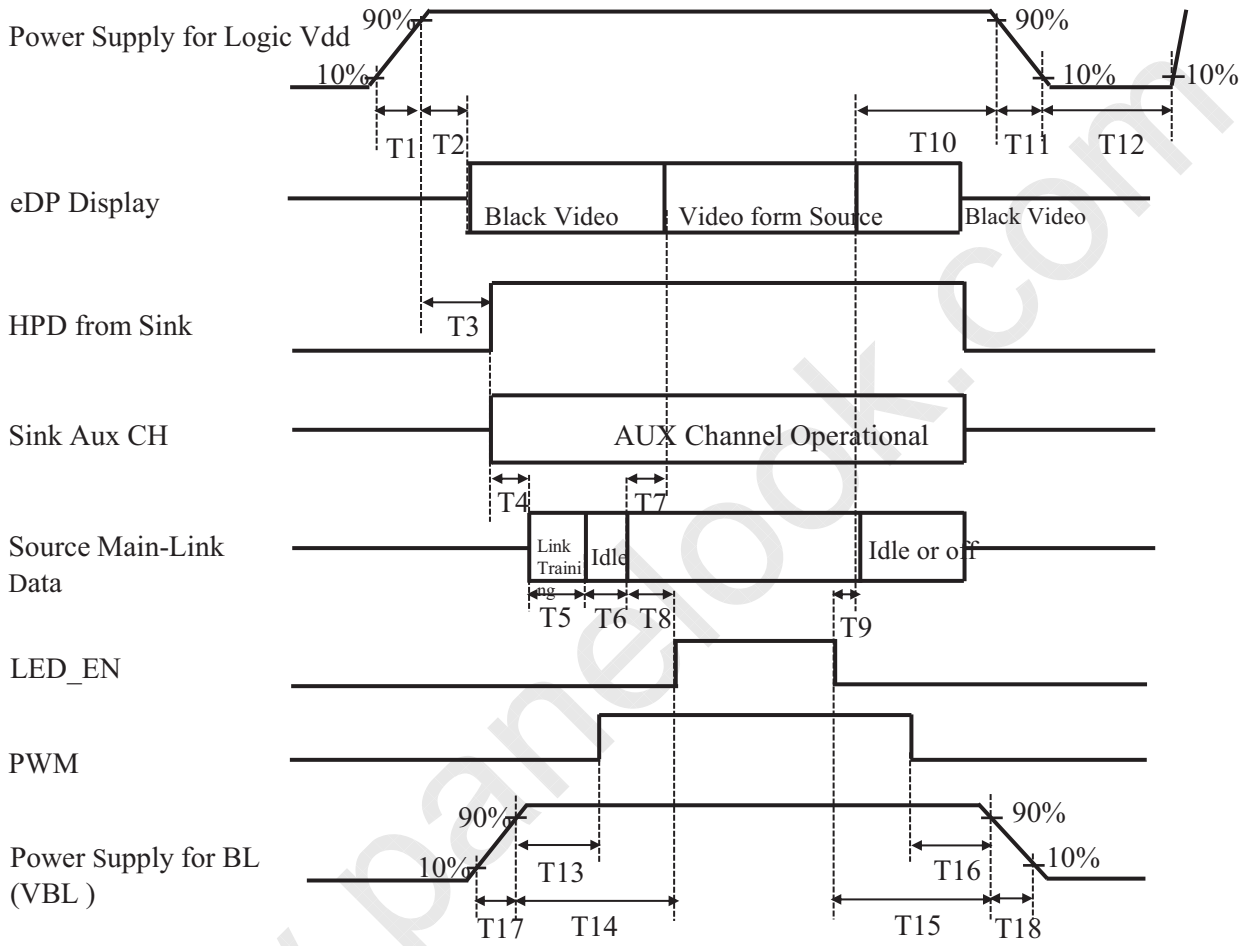


Figure 15. Power Sequence

- 0.5ms ≤ T1 ≤ 10 ms
- 0ms ≤ T2 ≤ 200 ms
- 0ms ≤ T3 ≤ 200 ms
- 10ms ≤ T13
- 20ms ≤ T14
- 0.5ms ≤ T17 ≤ 20ms
- T3+T4+T5+T6+T8>200ms
- 0ms ≤ T7 ≤ 50ms
- 0ms < T9
- 0ms ≤ T10 ≤ 500 ms
- 3ms ≤ T11 ≤ 10 ms
- 500ms ≤ T12
- 20ms ≤ T15
- 10ms ≤ T16
- 0.5ms ≤ T18 ≤ 20ms
- 50ms < T8

Notes:

1. When the power supply VDD is 0V, keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on. Back Light must be turn on after power for logic and interface signal are valid.

9.0 Connector Description

Physical interface is described as for the connector on LCM.
These connectors are capable of accommodating the following signals and will be following components.

9.1 TFT LCD Module

< Table 12. Signal Connector >

Connector Name /Description	For Signal Connector
Manufacturer	I-PEX
Type/ Part Number	20455-040E
Mating Housing/ Part Number	20455-040E-66

10.0 MECHANICAL CHARACTERISTICS

10.1 Dimensional Requirements

Figure 23 shows mechanical outlines for the model NV156FHM-T01 V8.0.
Other parameters are shown in Table 13.

<Table 13. Dimensional Parameters>

Parameter	Specification	Unit
Active Area	344.16 (H) ×193.59 (V)	mm
Number of pixels	1920 (H) X 1080 (V) (1 pixel = R + G + B dots)	pixels
Pixel pitch	179.25 (H) X 179.25 (V)	um
Pixel arrangement	RGB Vertical stripe	
Display colors	262K(6bit)	
Display mode	Normally Black	
Dimensional outline	350.66(H) ×216.15(V) (W/PCB) ×3.2max(panel side) 3.4max(PCBA side)	mm
Weight	385 (max)	g

10.2 Mounting

See Figure 20.

10.3 Glare and Polarizer Hardness.

The surface of the LCD has an **glare** coating to maximize readability and hard coating to reduce scratching.

10.4 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance 50cm from the screen with an overhead light level of 350lux.

11.0 RELIABILITY TEST

The reliability test items and its conditions are shown in below.

<Table 14. Reliability Test>

No	Test Items	Conditions
1	High temperature storage test	Ta = 60˚C , 60%RH, 240 hrs
2	Low temperature storage test	Ta = -20˚C , 240 hrs
3	High temperature & high humidity operation test	Ta = 50˚C , 80%RH, 240 hrs
4	High temperature operation test	Ta = 50˚C , 60%RH, 240 hrs
5	Low temperature operation test	Ta = 0˚C , 240 hrs
6	Thermal shock	Ta = -20 ˚C ↔ 60 ˚C (0.5 hr), 60%±3%RH, 100 cycle
7	Vibration test (non-operating)	Ta = 25˚C , 60%RH, 1.5G, 10~500Hz, Half Sine X,Y,Z / Sweep rate : 1 hour
8	Shock test (non-operating)	Ta = 25˚C , 60%RH, 220G, Half Sine Wave 2msec ± X, ± Y, ± Z Once for each direction
9	Electro-static discharge test (non-operating)	Air : 150 pF, 330Ω, 15 KV Contact : 150 pF, 330Ω, 8 KV Ta = 25˚C , 60%RH,

12.0 HANDLING & CAUTIONS

(1) Cautions when taking out the module
- Pick the pouch only, when taking out module from a shipping package.

(2) Cautions for handling the module
- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

(3) Cautions for the operation
- When the module is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

(4) Cautions for the atmosphere
- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

(5) Cautions for the module characteristics
- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

(6) Other cautions
- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc. Please pack the module not to be broken. We recommend to use the original shipping packages.

13.0 LABEL

(1) Product Label

Figure 16. Product Label

Module ID Naming Rule:

<Table 15. Module ID Naming Rule>

Digit / Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Code	S	L	S	5	1	2	3	5	9	4	2	0	0	0	1	D	B
Description	Model Code /GBN		Grade	Line	Year		Month	Model Extension Code (Last 4 Digits Of FGCOD)				Serial No 00001-ZZZZZZ					

(2) High voltage caution label

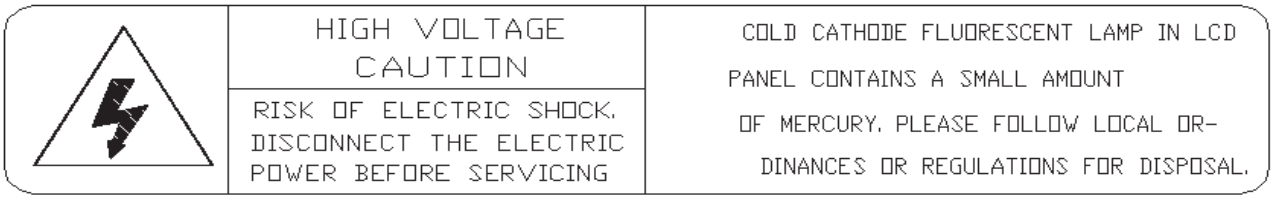


Figure 17. High Voltage Caution Label

(3) Box Label

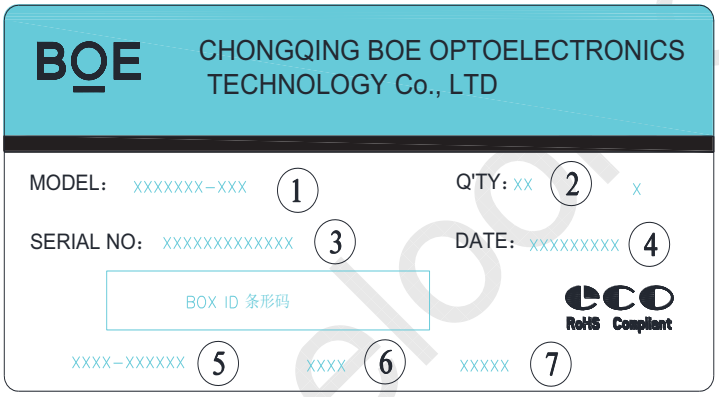


Figure 18. Box Label

Serial number marked part needs to print, show as follows:

1. FG-CODE(Before 12 bit)
2. Product quantity
3. Box ID
4. Date
5. The client section material number(The client)---XXXXXX-XXX
6. FG-Code After four ---8941
7. The supplier code
8. Total Size:100×50mm

<Table 16. Box Label Naming Rule >

Digit / Code	1	2	3	4	5	6	7	8	9	10	11	12	13
Code	S	L	S	F	1	2	3	D	0	0	0	6	8
Description	Products GBN		Grade	Line	Year		Month	Revision Code	Serial No				

14.0 PACKING INFORMATION

14.1 Packing Order

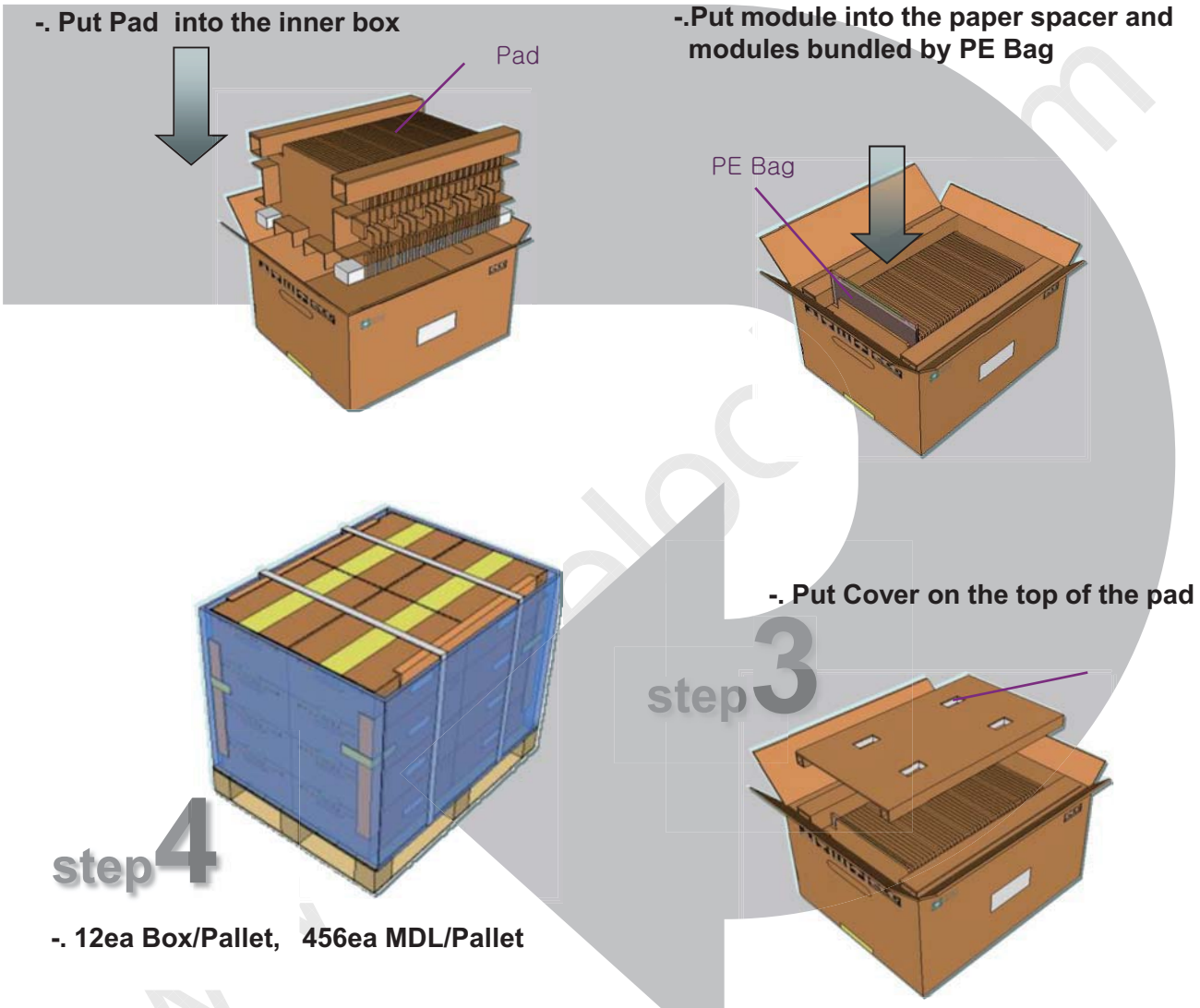


Figure 19. Packing Order

14.2 Note

- Box dimension: 480mm*350mm*285mm
- Package quantity in one box: 38pcs
- Total weight: 18.2kg/Box

15.0 MECHANICAL OUTLINE DIMENSION

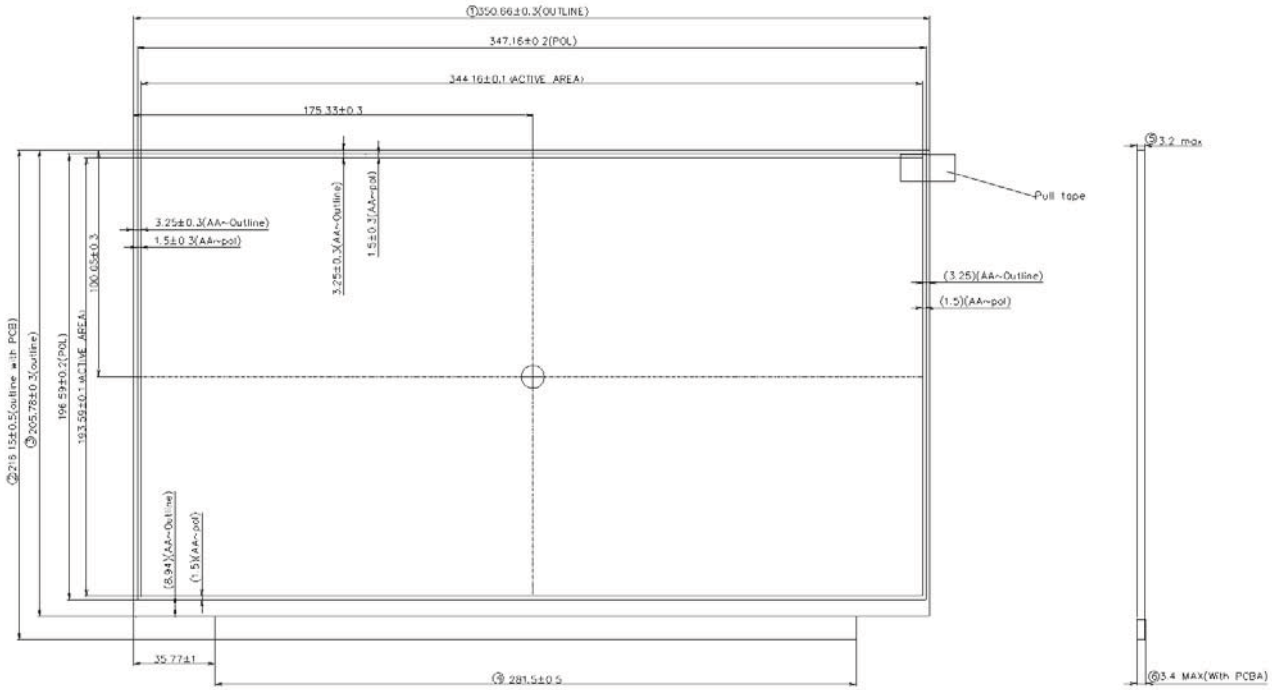


Figure 20. TFT-LCD Module Outline Dimension (Front View)

Note:

1. Warps And Deformation spec 0.5mm Max.
2. EDP connector is measured at PIN 1 and MATING LINE.
3. Key dimensions: ① -⑧
4. The MDL dimensions measure tool is Vernier Caliper.
5. Top Pol must be the highest portion in bottom including PCBA.

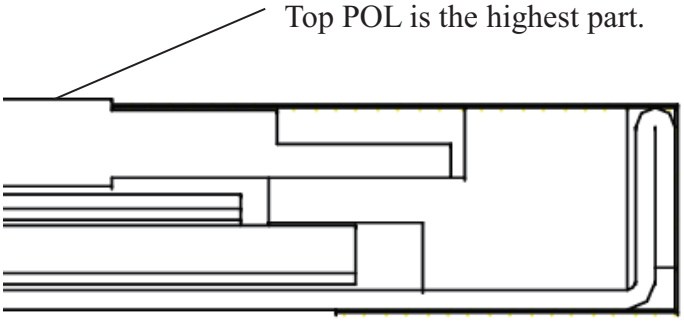


Figure 21. Highest Point Position

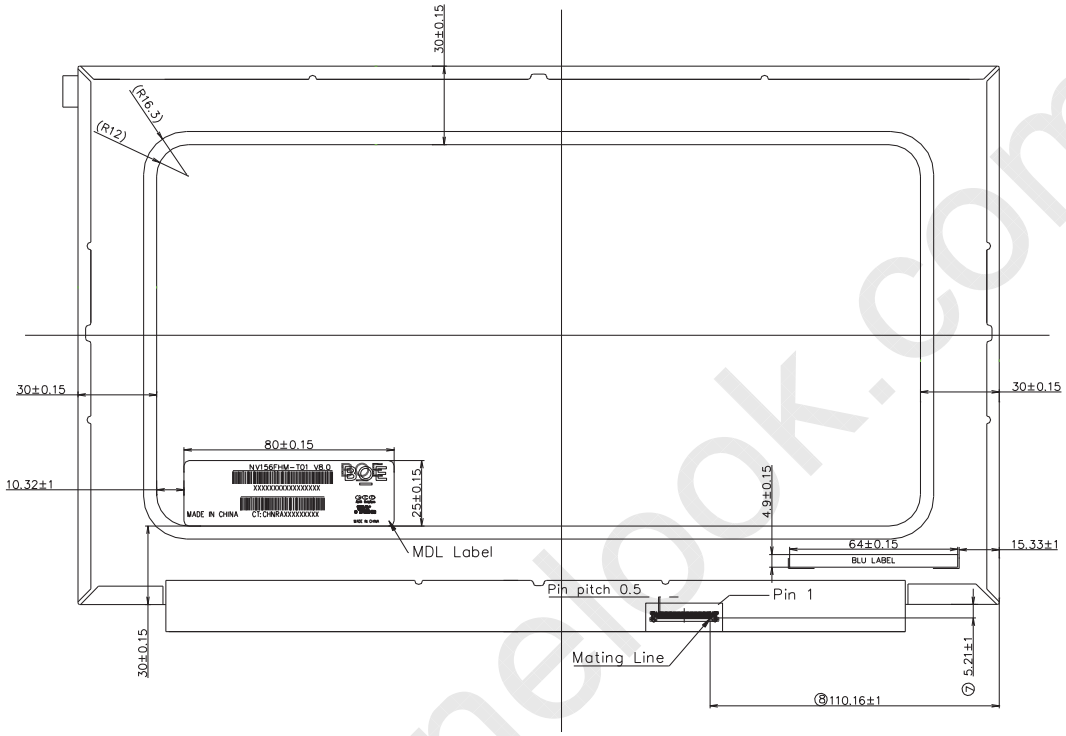


Figure 22. TFT-LCD Module Outline Dimensions (Rear view)

Note:
1. Warps And Deformation spec 0.5mm Max.
2. EDP connector is measured at PIN 1 and MATING LINE.
3. Key dimensions: ① -⑧
4. The MDL dimensions measure tool is Vernier Caliper.
5. Top Pol must be the highest portion in bottom including PCBA.

16.0 EDID Table

Address (HEX)	Function	Hex	Dec	crc	Input values.	Notes
00	Header	00	0		0	EDID Header
01		FF	255		255	
02		FF	255		255	
03		FF	255		255	
04		FF	255		255	
05		FF	255		255	
06		FF	255		255	
07		00	0		0	
08	ID Manufacturer Name	09	9		BOE	ID = BOE
09		E5	229			
0A	ID Product Code	80	128		1920	ID = 1920
0B		07	7			
0C	32-bit serial No.	00	0		0	
0D		00	0		0	
0E		00	0		0	
0F		00	0		0	
10	Week of manufacture	01	1		1	
11	Year of Manufacture	1B	27		2017	Manufactured in 2017
12	EDID Structure Ver.	01	1		1	EDID Ver 1.0
13	EDID revision #	04	4		4	EDID Rev. 0.4
14	Video input definition	95	149		-	Refer to right table
15	Max H image size	22	34		34	34 cm (Approx)
16	Max V image size	13	19		19	19 cm (Approx)
17	Display Gamma	78	120		2.2	Gamma curve = 2.2
18	Feature support	02	2		-	Refer to right table
19	Red/Green low bits	C9	201		-	Red / Green Low Bits
1A	Blue/White low bits	A0	160		-	Blue / White Low Bits
1B	Red x high bits	95	149	599	0.585	Red (x) = 10100101 (0.585)
1C	Red y high bits	5D	93	372	0.364	Red (y) = 01010101 (0.364)
1D	Green x high bits	59	89	358	0.350	Green (x) = 01001110 (0350)
1E	Green y high bits	94	148	593	0.580	Green (y) = 10011100 (0.580)
1F	Blue x high bits	29	41	166	0.163	Blue (x) = 00100110 (0.163)
20	BLue y high bits	24	36	146	0.143	Blue (y) = 00010000 (0.143)
21	White x high bits	50	80	320	0.313	White (x) = 01010000 (0.313)
22	White y high bits	54	84	336	0.329	White (y) = 01010100 (0.329)
23	Established timing 1	00	0		-	Refer to right table
24	Established timing 2	00	0		-	
25	Established timing 3	00	0		-	

26	Standard timing #1	01	1			Not Used
27		01	1			
28	Standard timing #2	01	1			Not Used
29		01	1			
2A	Standard timing #3	01	1			Not Used
2B		01	1			
2C	Standard timing #4	01	1			Not Used
2D		01	1			
2E	Standard timing #5	01	1			Not Used
2F		01	1			
30	Standard timing #6	01	1			Not Used
31		01	1			
32	Standard timing #7	01	1			Not Used
33		01	1			
34	Standard timing #8	01	1			Not Used
35		01	1			
36	Detailed timing/monitor descriptor #1	3C	60		141.4	141.4MHz Main clock
37		37	55			
38		80	128		1920	Hor Active = 1920
39		DE	222		222	Hor Blanking = 222
3A		70	112		-	4 bits of Hor. Active + 4 bits of Hor. Blanking
3B		38	56		1080	Ver Active = 1080
3C		14	20		20	Ver Blanking = 20
3D		40	64		-	4 bits of Ver. Active + 4 bits of Ver. Blanking
3E		30	48		48	Hor Sync Offset = 48
3F		20	32		32	H Sync Pulse Width = 32
40		36	54		3	V sync Offset = 3 line
41		00	0		6	V Sync Pulse width : 6 line
42		58	88		344	Horizontal Image Size = 381.888 mm (Low 8 bits)
43		C2	194		194	Vertical Image Size = 214.812 mm (Low 8 bits)
44		10	16		-	4 bits of Hor Image Size + 4 bits of Ver Image Size
45		00	0		0	Hor Border (pixels)
46		00	0		0	Vertical Border (Lines)
47		1A	26		-	Refer to right table

48	Detailed timing/monitor descriptor #2	52	82		98.1	98.1MHz Main clock
49		26	38			
4A		80	128		1920	Hor Active = 1920
4B		0E	14		270	Hor Blanking = 270
4C		71	113		-	4 bits of Hor. Active + 4 bits of Hor. Blanking
4D		38	56		1080	Ver Active = 1080
4E		28	40		40	Ver Blanking = 40
4F		40	64		-	4 bits of Ver. Active + 4 bits of Ver. Blanking
50		30	48		48	Hor Sync Offset = 48
51		20	32		32	H Sync Pulse Width = 32
52		36	54		3	V sync Offset = 3 line
53		00	0		6	V Sync Pulse width : 6 line
54		58	88		344	Horizontal Image Size = 344 mm (Low 8 bits)
55		C2	194		194	Vertical Image Size = 194 mm (Low 8 bits)
56		10	16		-	4 bits of Hor Image Size + 4 bits of Ver Image Size
57		00	0		0	Hor Border (pixels)
58		00	0		0	Vertical Border (Lines)
59		1A	26		-	Refer to right above table
5A	Detailed timing/monitor descriptor #3	00	0			Nvidia nvDPS (Refer the tab of nvDPS) Lowest refresh rate that does not cause any visual/optical side effect
5B		00	0			
5C		00	0			
5D		00	0			
5E		00	0			
5F		00	0			
60		00	0			
61		00	0			
62		00	0			
63		00	0			
64		00	0			
65		00	0			
66		00	0			
67		00	0			
68		00	0			
69		00	0			
6A		00	0			
6B		00	0			

6C	Detailed timing/monitor descriptor #4	00	0			Detailed Timing Description #4
6D		00	0			Flag
6E		00	0			Reserved
6F		02	2			For Brightness Table and Power consumption
70		00	0			Flag
71		0A	10		-	PWM % [7:0] @ Step 0
72		3D	61		-	PWM % [7:0] @ Step 5
73		FF	255		-	PWM % [7:0] @ step 10
74		0A	10		-	Nits [7:0] @ Step 0
75		3C	60		-	Nits [7:0] @ Step 5
76		7D	125		-	Nits [7:0] @ Step 10
77		12	18		-	Panel Electronics Power @32x32 Chess Pattern = 729mW
78		13	19		-	Backlight Power @60 nits = 768mW
79		26	38		-	Backlight Power @Step 10 = 3100mW
7A		7D	125		-	Nits @ 100% PWM Duty = 250nit
7B		00	0			Format： terminate with ASCII code 0Ah and pad field with ASCII code 20h
7C		00	0			
7D		00	0			
7E	Extension flag	00	0		1	0 ：1個EDID；N-1：N个EDID
7F	Checksum	**98**	**152**	**152**	-	