Doc. Number:

☐ Tentative Specification
☐ Preliminary Specification
■ Approval Specification

MODEL NO.: N156HCA
SUFFIX: EAB Rev.C2

Customer: ASUS

APPROVED BY **SIGNATURE**

Name / Title

Note：

Please return 1 copy for your confirmation with your signature and comments.

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CONTENTS

1. GENERAL DESCRIPTION 4
1.1 OVERVIEW 4
2. MECHANICAL SPECIFICATIONS 5
2.1 CONNECTOR TYPE 5
3. ABSOLUTE MAXIMUM RATINGS 6
3.1 ABSOLUTE RATINGS OF ENVIRONMENT 6
3.2 ELECTRICAL ABSOLUTE RATINGS 7
3.2.1 TFT LCD MODULE 7
4. ELECTRICAL SPECIFICATIONS 8
4.1 FUNCTION BLOCK DIAGRAM 8
4.2. INTERFACE CONNECTIONS 8
4.3 ELECTRICAL CHARACTERISTICS 10
4.3.1 LCD ELETRONICS SPECIFICATION 10
4.3.2 LED CONVERTER SPECIFICATION 12
4.3.3 BACKLIGHT UNIT 14
4.4 DISPLAY PORT INPUT SIGNAL TIMING SPECIFICATIONS 15
4.4.1 DISPLAY PORT INTERFACE 15
4.5 DISPLAY TIMING SPECIFICATIONS 16
4.6 POWER ON/OFF SEQUENCE 17
5. OPTICAL CHARACTERISTICS 20
5.1 TEST CONDITIONS 20
5.2 OPTICAL SPECIFICATIONS 20
6. RELIABILITY TEST ITEM 24
7. PACKING 25
7.1 MODULE LABEL 25
7.2 CARTON 26
7.3 PALLET 27
7.4 UN-PACKAGING METHOD 28
8. PRECAUTIONS 29
8.1 HANDLING PRECAUTIONS 29
8.2 STORAGE PRECAUTIONS 29
8.3 OPERATION PRECAUTIONS 29
Appendix. EDID DATA STRUCTURE 30
Appendix. OUTLINE DRAWING 33
Appendix. SYSTEM COVER DESIGN GUIDANCE 37
Appendix. LCD MODULE HANDLING MANUAL 46

REVISION HISTORY

Version	Date	Page	Description
0.0	Oct. 27, 2020	All	Spec Ver.0.0 was first issued.
0.1	Dec. 04, 2020	All	Spec Ver.0.1 was first issued.
		10	4.3.1 LCD ELETRONICS SPECIFICATION Ripple Voltage was updated
		33~35	Appendix. OUTLINE DRAWING was updated
		36~43	Appendix. SYSTEM COVER DESIGN GUIDANCE was updated
1.0	Jan.06, 2021	All	Spec Ver.1.0 was first issued.
		4	1.2 GENERAL SPECIFICATI0NS of Special Function was updated
		25	7.1 MODULE LABEL of INX Version from xx change to C2
		30~32	Appendix. EDID DATA STRUCTURE was updated
		33	Appendix. OUTLINE DRAWING was updated
1.1	Jan.14, 2021	All	Spec Ver.1.1 was first issued.
		10	4.3.1 LCD ELETRONICS SPECIFICATION add Note(6) for Ripple Voltage
3.0	Jan.26, 2021	All	Spec Ver.3.0 was first issued.
		10	The Mosaic and Black pattern of Power Supply Current was updated in 4.3.1 LCD ELETRONICS SPECIFICATION
3.1	May.06, 2021	All	Spec Ver.3.1 was first issued.
		5	2.1 CONNECTOR TYPE was updated
3.2	Dec.21, 2021	All	Spec Ver.3.1 was first issued.
		30~32	Appendix. EDID DATA STRUCTURE was updated by Byte 53~63
3.3	May,10, 2022	All	Spec Ver.3.6 was first issued.
		12	4.3.2 LED CONVERTER SPECIFICATION of Converter Inrush Current was updated

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N156HCA-EAB is a 15.6" (15.547" diagonal) TFT Liquid Crystal Display NB module with LED Backlight unit and 30 pins eDP interface. This module supports 1920 x 1080 FHD AAS mode and can display 16.7M colors.

1.2 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Screen Size	15.6" diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1080	pixel	-
Pixel Pitch	0.17925 (H) x 0.17925 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16,777,216	color	-
Color depth	6bit+Hi-FRC		
Transmissive Mode	Normally Black	-	-
Surface Treatment	Hard coating (3H), Anti-Glare	-	-
Color Gamut	45%	NTSC	typ
Luminance, White	250	Cd/m2	
Response Time	Typ:T_R 14 / T_F 11	ms	
Contrast Ratio	Typ:1000/Min:800		
Border size(L/R/U)	3.25/3.25/3.25	mm	
View Angle(U/D/R/L)	89/89/89/89	Deg	
Blacklight Unit	40LEDs,strings 10, parallel 4		
Electrical Interface	eDP1.2		
RoHs Compliance	Yes		
Power Consumption	Total 4.158 W (Max.)@cell 0.858 W (Max.), BL 3.3W(Max.)		
Special Function	G-sync DD (Not support) G-sync nVSR (Not support) Free-sync (Not support) Static DRRS (Not support) Seamless DRRS(sDRRS) Not support) PSR Version(PSR1 or PSR2) (Not support) PSR 1+ sDRRS(Not support) PSR 2+ LRR(Not support) CABC(Not support)		

Note (1) The specified power consumption (with converter efficiency) is under the conditions at VCCS = 3.3 V, fv = 60 Hz, LED_VCCS = Typ, fPWM = 200 Hz, Duty=100% and Ta = 25 ± 2 ºC, whereas mosaic pattern is displayed.

Note (2) Display port interface signals should follow VESA DisplayPort Standard Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.2 (eDP1.2). There are many optional items described in eDP1.2. If some optional item is requested, please contact us.

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	350.36	350.66	350.96	mm	(1) (2)
	Vertical (V)	204.95	205.25	205.55	mm	
	Thickness (T)	-	3.05	3.20	mm	
Active Area	Horizontal	-	344.16	-	mm	
	Vertical	-	193.59	-	mm	
Weight		-	350	365	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Dimensions are measured by caliper.

2.1 CONNECTOR TYPE

Please refer Appendix Outline Drawing for detail design.

Connector Part No.: 1st IPEX-20455-030E-12 , 2nd JAE-HD2S030HA3

or follow customer approval connector vender list

User's connector Part No: I-PEX-20453-030E-03

Customer approval connector vender list

Item	Discription				
LCD Panel Connector Pool	Item	Pin 數	Pitch	廠商	廠商料號
	1	40	0.5	I-PEX	**20455-040E-02/12**
					20455-040E-76/66
					20765-040E-11
				Starconn	111A40-0000RA-G3
				STM	**MSAK24025P40**
				Tyco	5-2069716-3
				LSMtrom	GT05Q-40S-10H
				Foxconn	GS13401-1S10S-7H
				JAE	HD1S040HA1
					HD1S040HA2
					HD1S040HA3
				UJU	IS050-L40B-C10
				MOLEX	MOLEX-104062-4011
	2	30	0.5	I-PEX	**20455-030E-02/12**
					20455-030E-76/66
					20765-030E-11
				Starconn	300E30-0010RA-G3
				JAE	HD2S030HA1
					HD2S030HA2
					HD2S030HA3
				LSMtrom	GT05Q-30S-H10-MN
				STM	**MSAK24025P30**
				UJU	IS050-L30B-C10
	3	40	0.4	I-PEX	20682-040E-02

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

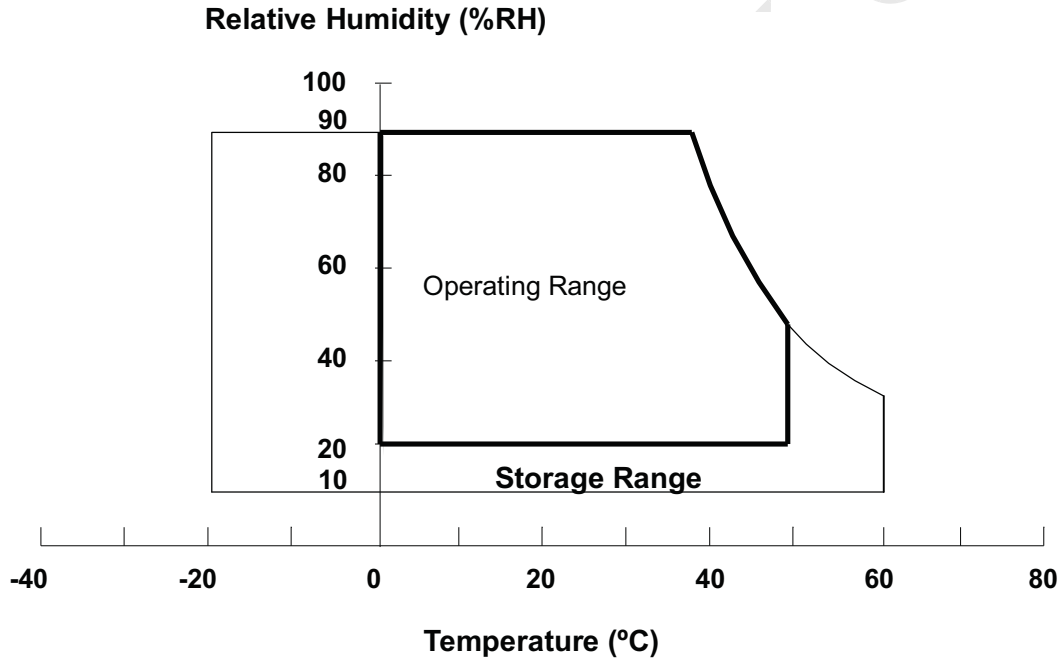
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	--	220/2	G/ms	(3),(4),(5)
Vibration (Non-Operating)	V_{NOP}	--	1.5	G	(3),(4),(6)

Note (1) (a) 90 %RH Max. (Ta < 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max.

(c) No condensation.

Note (2) The temperature of panel surface should be 0 ºC min. and 60 ºC max.



Note (3) criteria: Normal display image with no obvious non-uniformity and no line defect.

Note (4) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

Note (5) half sine wave,1 time for each direction of ±X,±Y,±Z

Note (6) 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z

3.2 ELECTRICAL ABSOLUTE RATINGS

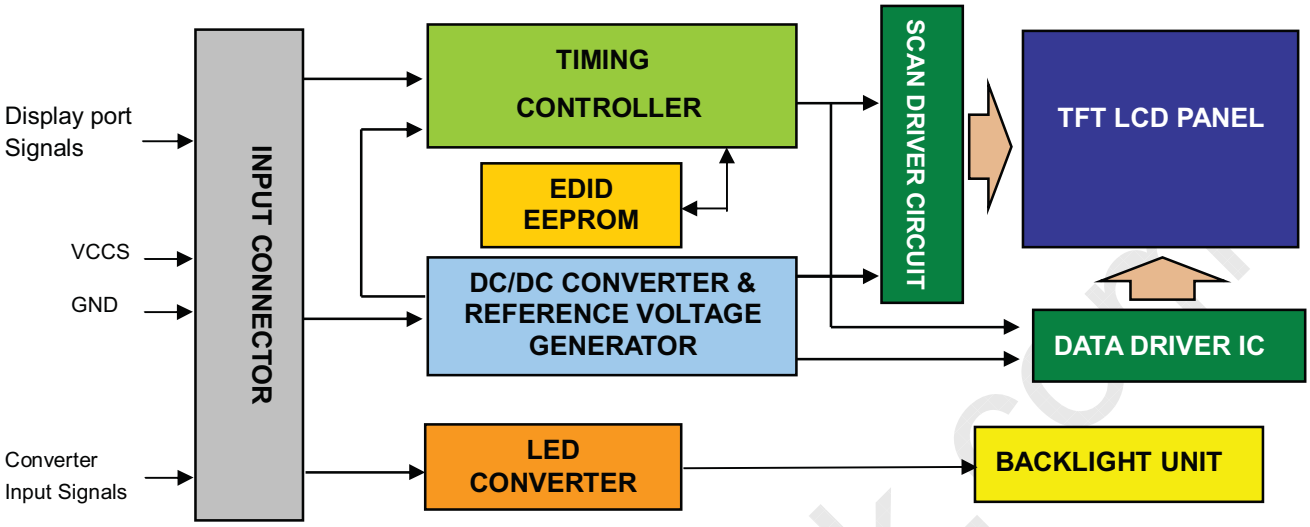
3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	VCCS+0.3	V	
Converter Input Voltage	LED_VCCS	-0.3	26	V	(1)
Converter Control Signal Voltage	LED_PWM,	-0.3	5	V	1)
Converter Control Signal Voltage	LED_EN	-0.3	5	V	(1)

Note (1) Stresses beyond those listed in above “ELECTRICAL ABSOLUTE RATINGS” may cause permanent damage to the device. Normal operation should be restricted to the conditions described in “ELECTRICAL CHARACTERISTICS”.

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



4.2. INTERFACE CONNECTIONS

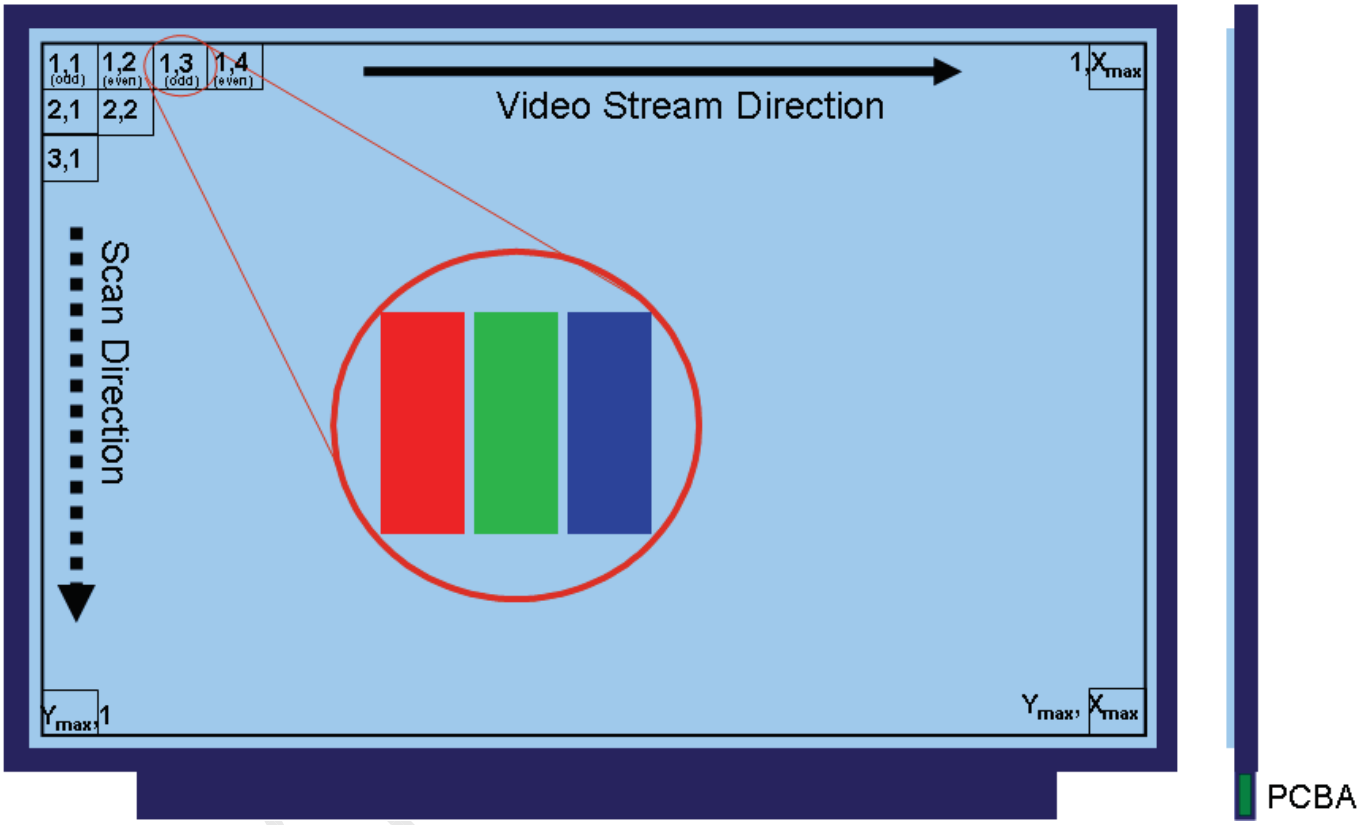
PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	NC	No Connection (Reserved for LCD test)	
2	H_GND	High Speed Ground	
3	ML1-	Complement Signal-Lane 1	
4	ML1+	True Signal-Main Lane 1	
5	H_GND	High Speed Ground	
6	ML0-	Complement Signal-Lane 0	
7	ML0+	True Signal-Main Lane 0	
8	H_GND	High Speed Ground	
9	AUX+	True Signal-Auxiliary Channel	
10	AUX-	Complement Signal-Auxiliary Channel	
11	H_GND	High Speed Ground	
12	VCCS	Power Supply +3.3 V (typical)	
13	VCCS	Power Supply +3.3 V (typical)	
14	NC	No Connection (Reserved for LCD test)	
15	GND	Ground	
16	GND	Ground	
17	HPD	Hot Plug Detect	
18	BL_GND	BL Ground	
19	BL_GND	BL Ground	
20	BL_GND	BL Ground	
21	BL_GND	BL Ground	
22	LED_EN	BL_Enable Signal of LED Converter	
23	LED_PWM	PWM Dimming Control Signal of LED Converter	
24	NC	No Connection (Reserved for LCD test)	
25	NC	No Connection (Reserved for LCD test)	

26	LED_VCCS	BL Power	
27	LED_VCCS	BL Power	
28	LED_VCCS	BL Power	
29	LED_VCCS	BL Power	
30	NC	No Connection (Reserved for INNOLUX test)	

f

Note (1) The first pixel is odd as shown in the following figure.



4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

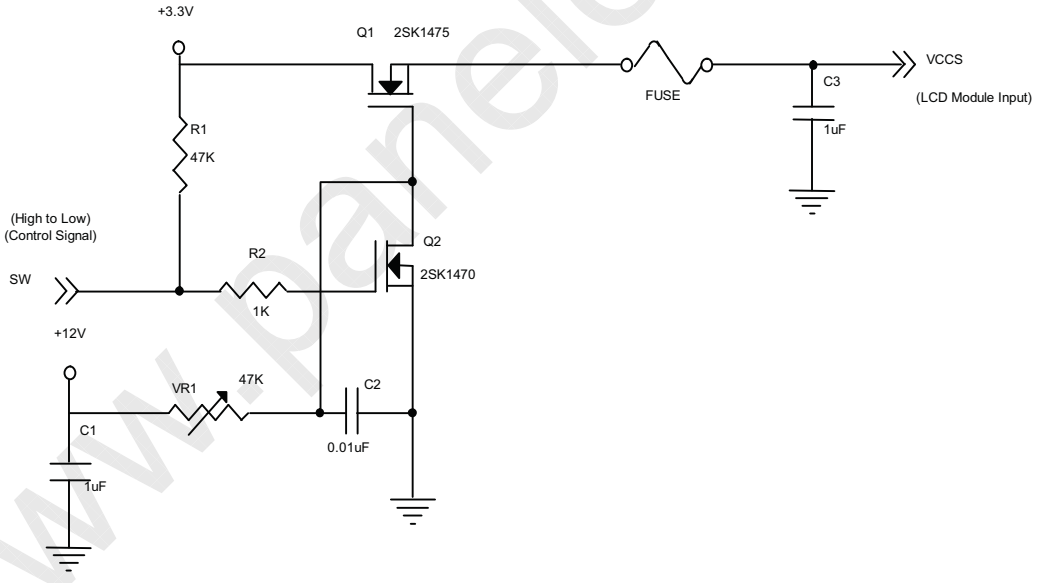
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)-
Ripple Voltage		V_{RP}	-	-	100	mV	(1),(6)
Inrush Current		I_{RUSH}	-	-	1.5	A	(1),(2)
Power Supply Current	Black	Icc		220	250	mA	(3)
	Mosaic			225	260	mA	(3)a
	Solid Pattern			400	450	mA	(3)b
HPD Impedance		R_{HPD}	30K			ohm	(4)
HPD	High Level		2.25	-	3.6	V	(5)
	Low Level		0	-	0.4	V	(5)

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

Note (2) I_{RUSH}: the maximum current when VCCS is rising

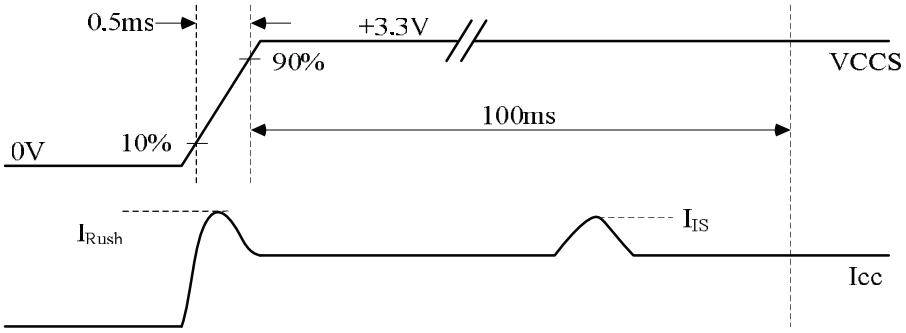
I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.



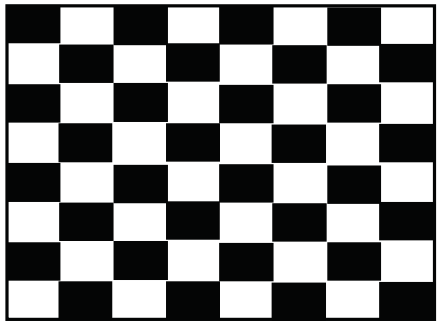
VCCS r-eDP Display

0.5ms



Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 ºC, DC Current and f_v = 60 Hz, whereas a specified power dissipation check pattern is displayed

a. Mosaic Pattern



Active Area

b. The solid pattern is the largest one of R/G/B pattern.

Note (4) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. Please refer to Note (4) of 4.3.2 LED CONVERTER SPECIFICATION to obtain more information.

Note (5) When a source detects a low-going HPD pulse, it must be regarded as a HPD event. Thus, the source must read the link / sink status field or receiver capability field of the DPCD and take corrective action.

Note (6) The VCCS voltage drop will occur at the frame start. We only consider the ripple voltage during active area instead of the blanking area. Meanwhile,the min VCCS need to meet “Power Supply Voltage” criteria.

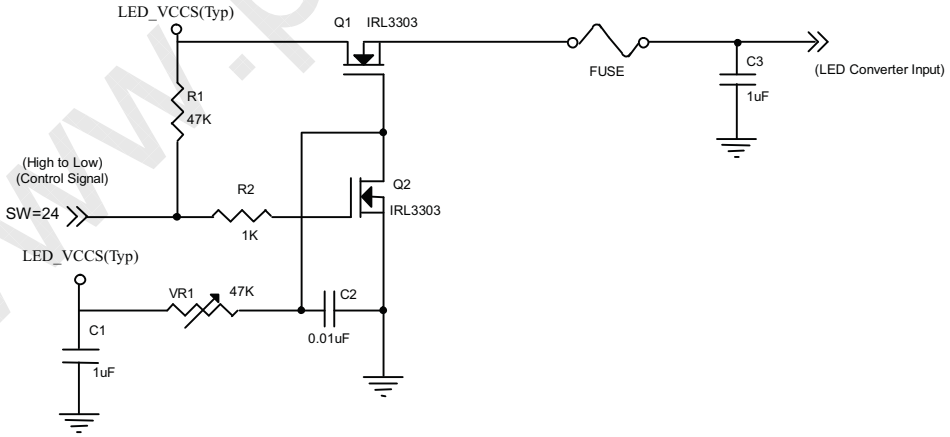
4.3.2 LED CONVERTER SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input power supply voltage		LED_Vccs	5.0	12.0	21.0	V	
Converter Inrush Current		$ILED_{RUSH}$	-	0.914	1.097	A	(1)
LED_EN Control Level	Backlight On		2.2	-	5.0	V	(4)
	Backlight Off		0	-	0.6	V	(4)
LED_EN Impedance		R_{LED_EN}	30K -	-		ohm	(4)
PWM Control Level	PWM High Level		2.2	-	5	V	(4)
	PWM Low Level		0	-	0.6	V	(4)
PWM Impedance		R_{PWM}	30K -	-		ohm	(4)
PWM Control Duty Ratio			5	-	100	%	(5)
PWM Control Permissive Ripple Voltage		VPWM_pp	-	-	100	mV	
PWM Control Frequency		f_{PWM}	190	-	10K	Hz	(2)
LED Power Current	LED_VCCS =Typ.	ILED	-	262	275	mA	(3)

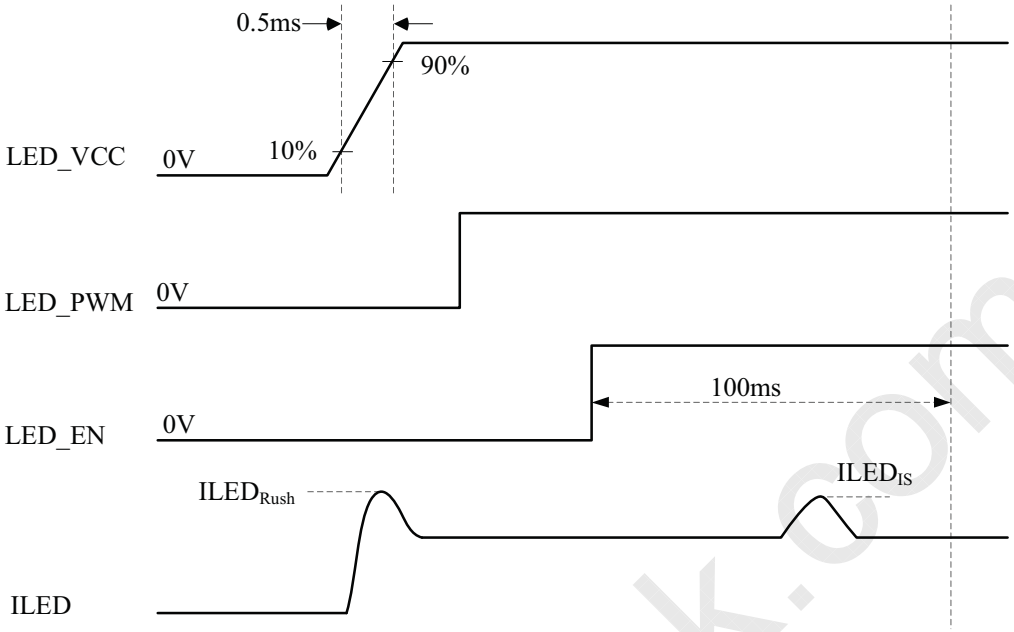
Note (1) $ILED_{RUSH}$: the maximum current when LED_VCCS is rising,

$ILED_{IS}$: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Min, Ta = 25 ± 2 ºC, Duty=100%,White pattern.



VLED rising time is 0.5ms



Note (2) If PWM control frequency is applied in the range less than 1KHz, the "waterfall" phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

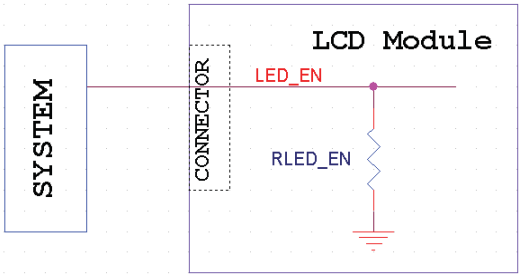
$$(N+0.33)*f \le f_{PWM} \le (N+0.66)*f$$

N : Integer $(N \ge 3)$

f : Frame rate

Note (3) The specified LED power supply current is under the conditions at "LED_VCCS = Typ.", Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.

Note (4) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. For example, the figure below describes the equivalent pull down impedance of LED_EN (If it exists). The rest pull down impedances of other signals (eg. HPD, PWM …) are in the same concept.



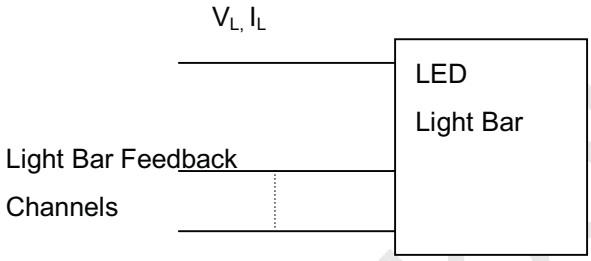
Note (5) If the cycle-to-cycle difference of PWM duty exceeds 0.1%, especially when the PWM duty is low, slight brightness change might be observed.

4.3.3 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V_L	26	29	30	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	I_L	-	90	-	mA	
Power Consumption	P_L	2.34	2.61	2.7	W	(3)
LED Life Time	L_{BL}	15000	-	-	Hrs	(4)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below :



Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) PL = IL ×VL (Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 oC and IL = 22.5mA (Per EA) until the brightness becomes ≦ 50% of its original value.

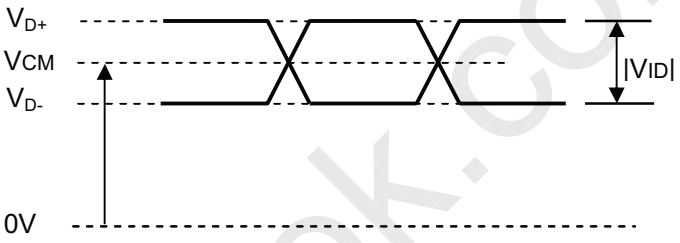
4.4 DISPLAY PORT INPUT SIGNAL TIMING SPECIFICATIONS

4.4.1 DISPLAY PORT INTERFACE

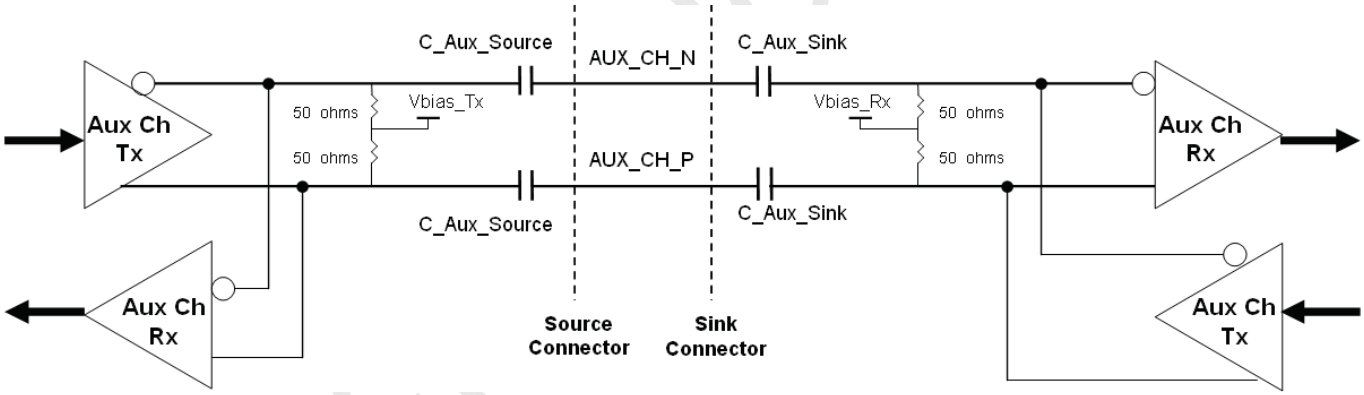
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Differential Signal Common Mode Voltage(MainLink and AUX)	VCM	0		2	V	(1) (4)
AUX AC Coupling Capacitor	C_Aux_Source	75		200	nF	(2)
Main Link AC Coupling Capacitor	C_ML_Source	75		200	nF	(3)

Note (1)Display port interface related AC coupled signals should follow VESA DisplayPort Standard Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.2. There are many optional items described in eDP1.2. If some optional item is requested, please contact us.

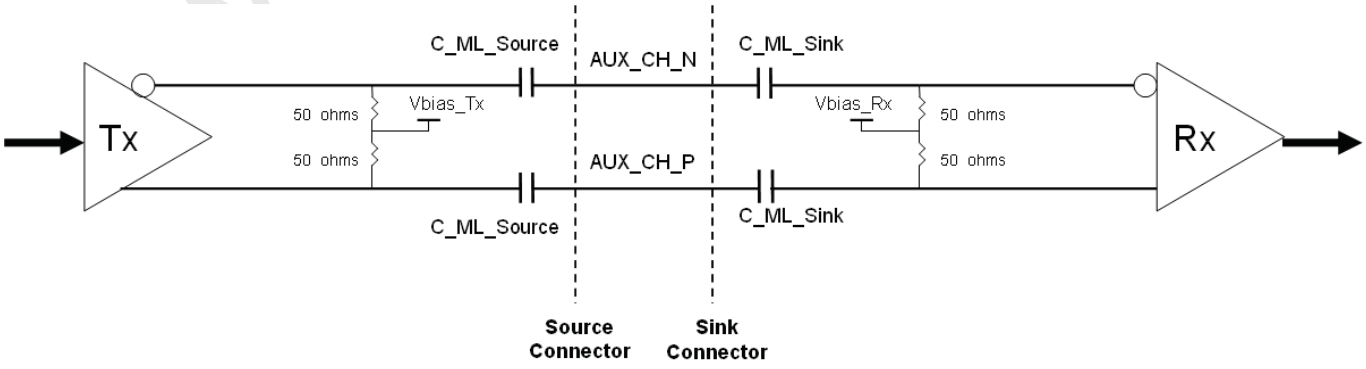
Single Ended



(2) Recommended eDP AUX Channel topology is as below and the AUX AC Coupling Capacitor (C_Aux_Source) should be placed on the source device.



(3) Recommended Main Link Channel topology is as below and the Main Link AC Coupling Capacitor (C_ML_Source) should be placed on the source device.



(4) The source device should pass the test criteria described in DisplayPortCompliance Test Specification (CTS) 1.1

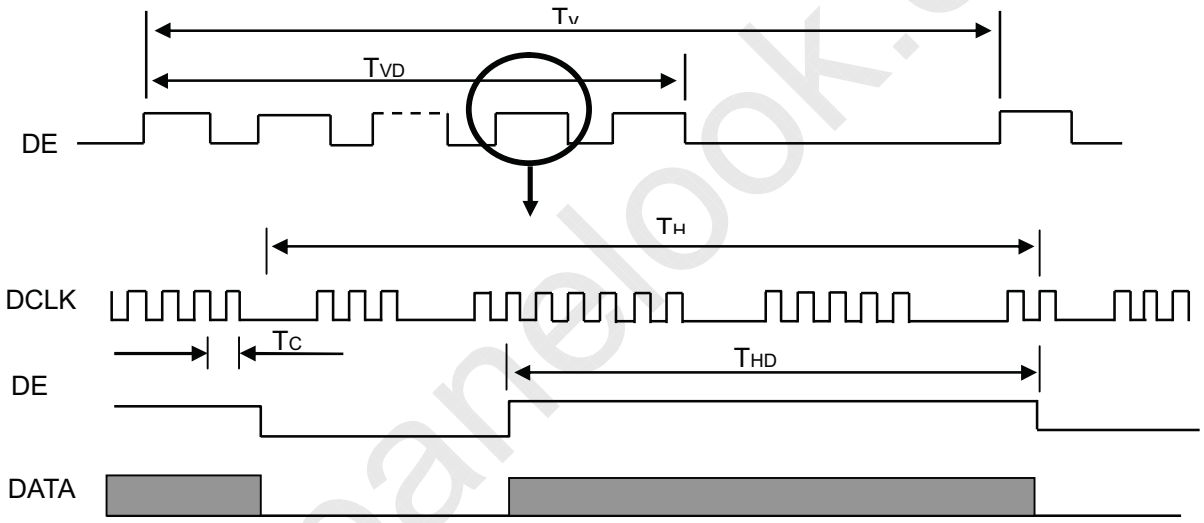
4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

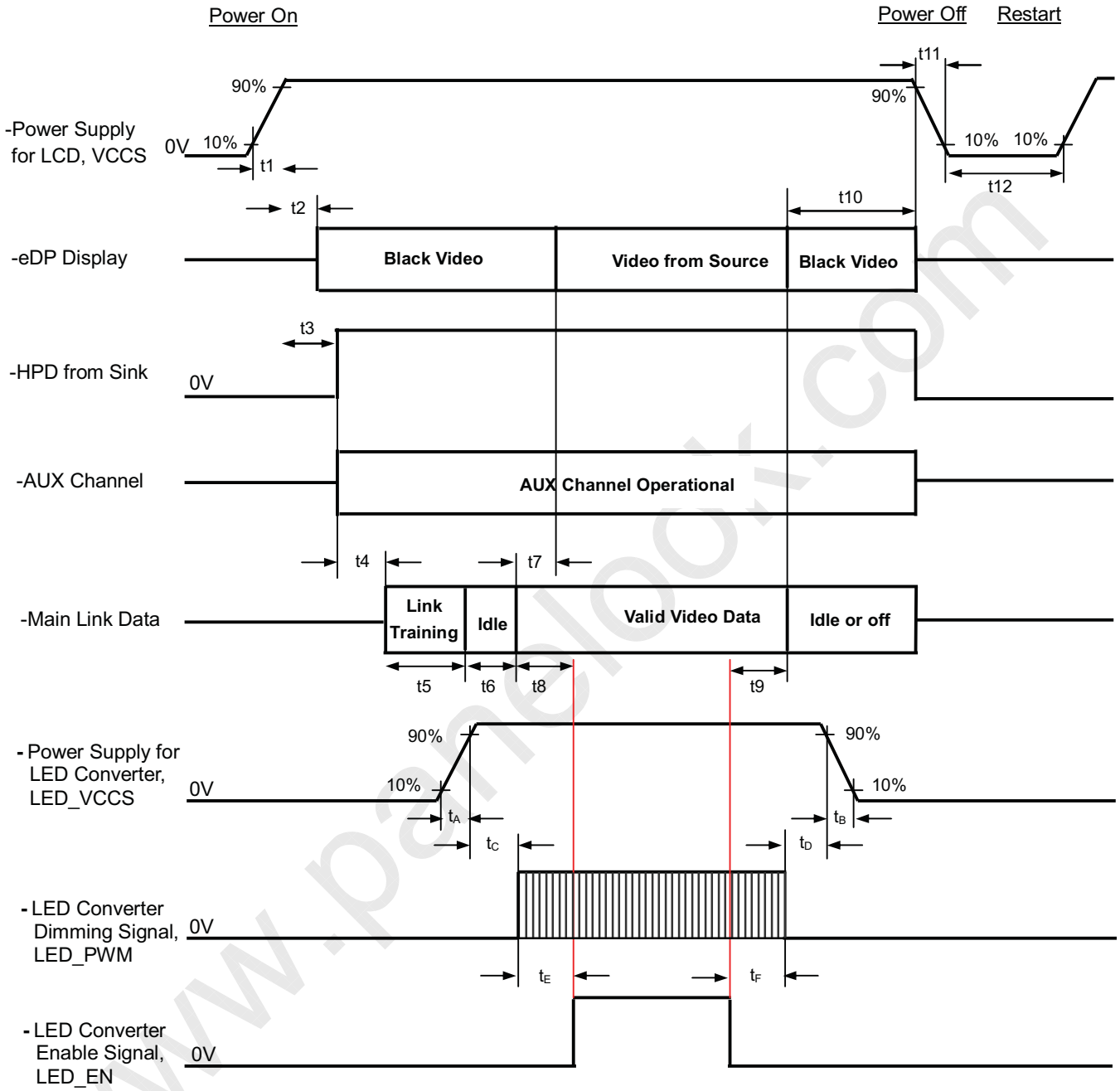
Refresh rate 60Hz

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	151.6	152.84	154.04	MHz	-
DE	Vertical Total Time	TV	1128	1132	1136	TH	-
	Vertical Active Display Period	TVD	1080	1080	1080	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	52	TV-TVD	TH	-
	Horizontal Total Time	TH	2230	2250	2260	Tc	-
	Horizontal Active Display Period	THD	1920	1920	1920	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	330	TH-THD	Tc	-

INPUT SIGNAL TIMING DIAGRAM



4.6 POWER ON/OFF SEQUENCE



Timing Specifications:

Parameter	Description	Reqd. By	Value		Unit	Notes
			Min	Max		
t1	Power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t2	Delay from LCD,VCCS to black video generation	Sink	0	200	ms	Automatic Black Video generation prevents display noise until valid video data is received from the Source (see Notes:2 and 3 below)
t3	Delay from LCD,VCCS to HPD high	Sink	0	200	ms	Sink AUX Channel must be operational upon HPD high (see Note:4 below)
t4	Delay from HPD high to link training initialization	Source	0	-	ms	Allows for Source to read Link capability and initialize
t5	Link training duration	Source	0	-	ms	Dependant on Source link training protocol
t6	Link idle	Source	0	-	ms	Min Accounts for required BS-Idle pattern. Max allows for Source frame synchronization
t7	Delay from valid video data from Source to video on display	Sink	0	50	ms	Max value allows for Sink to validate video data and timing. At the end of T7, Sink will indicate the detection of valid video data by setting the SINK_STATUS bit to logic 1 (DPCD 00205h, bit 0), and Sink will no longer generate automatic Black Video
t8	Delay from valid video data from Source to backlight on	Source	80*	-	ms	Source must assure display video is stable*: Recommended by INX. To avoid garbage image.
t9	Delay from backlight off to end of valid video data	Source	50*	-	ms	Source must assure backlight is no longer illuminated. At the end of T9, Sink will indicate the detection of no valid video data by setting the SINK_STATUS bit to logic 0 (DPCD 00205h, bit 0), and Sink will automatically display Black Video. (See Notes: 2 and 3 below) *: Recommended by INX. To avoid garbage image.
t10	Delay from end of valid video data from Source to power off	Source	0	500	ms	Black video will be displayed after receiving idle or off signals from Source
t11	VCCS power rail fall time, 90% to 10%	Source	0.5	10	ms	-
t12	VCCS Power off time	Source	500	-	ms	-
t_A	LED power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t_B	LED power rail fall time, 90% to 10%	Source	0	10	ms	-
t_C	Delay from LED power rising to LED dimming signal	Source	1	-	ms	-

t_D	Delay from LED dimming signal to LED power falling	Source	1	-	ms	-
t_E	Delay from LED dimming signal to LED enable signal	Source	0	-	ms	-
t_F	Delay from LED enable signal to LED dimming signal	Source	0	-	ms	-

Note (1) Please don't plug or unplug the interface cable when system is turned on.

Note (2) The Sink must include the ability to automatically generate Black Video autonomously. The Sink must automatically enable Black Video under the following conditions:

- Upon LCDVCC power-on (within T2 max)
- When the "NoVideoStream_Flag" (VB-ID Bit 3) is received from the Source (at the end of T9)

Note (3) The Sink may implement the ability to disable the automatic Black Video function, as described in Note (2), above, for system development and debugging purposes.

Note (4) The Sink must support AUX Channel polling by the Source immediately following LCDVCC power-on without causing damage to the Sink device (the Source can re-try if the Sink is not ready). The Sink must be able to response to an AUX Channel transaction with the time specified within T3 max.

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

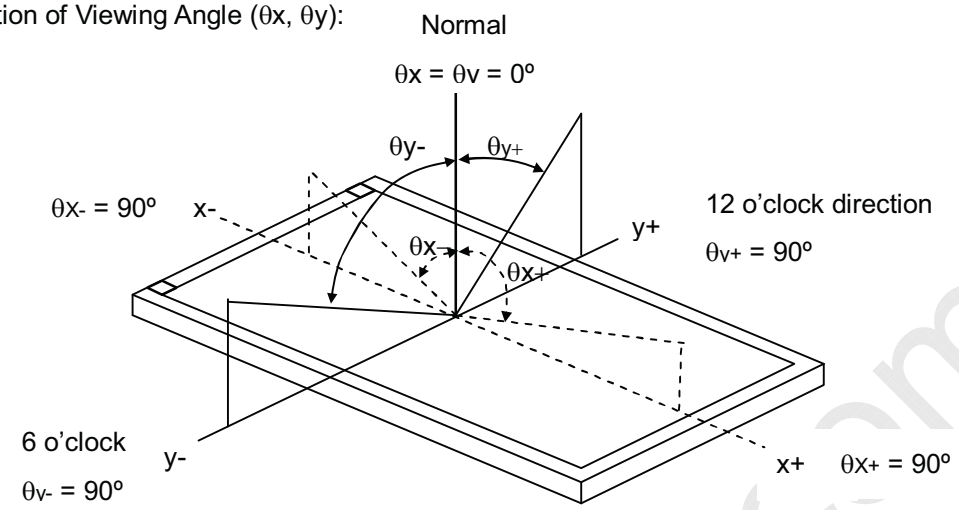
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I_L	90	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	800	1000	-	-	(2), (5),(7)
Response Time		T_R		-	14	16	ms	(3),(7)
		T_F		-	11	14	ms	
Average Luminance of White		L_{AVE}		212	250	-	cd/m^2	(4), (6),(7)
Color Chromaticity	Red	Rx	θ_x=0°, θ_Y =0° Viewing Normal Angle	Typ – 0.03	0.590	Typ + 0.03	-	(1),(7)
		Ry			0.350		-	
	Green	Gx			0.330		-	
		Gy			0.555		-	
	Blue	Bx			0.153		-	
		By			0.119		-	
	White	Wx			0.313		-	
		Wy			0.329		-	
NTSC		CG		42	45	-	%	(5),(7),(8)
Cross talk		CT		-	-	4	%	(5),(7),(9)
Viewing Angle	Horizontal	θ_x+	CR≥10	80	89	-	Deg.	(1),(5), (7)
		θ_x-		80	89	-		
	Vertical	θ_Y+		80	89	-		
		θ_Y-		80	89	-		
White Variation of 5 Points		δW_{5p}	θ_x=0°, θ_Y =0°	-	-	1.25	-	(5),(6), (7)
White Variation of 13 Points		δW_{13p}	θ_x=0°, θ_Y =0°	-	-	1.5		(5),(6), (7)

Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255 / L0

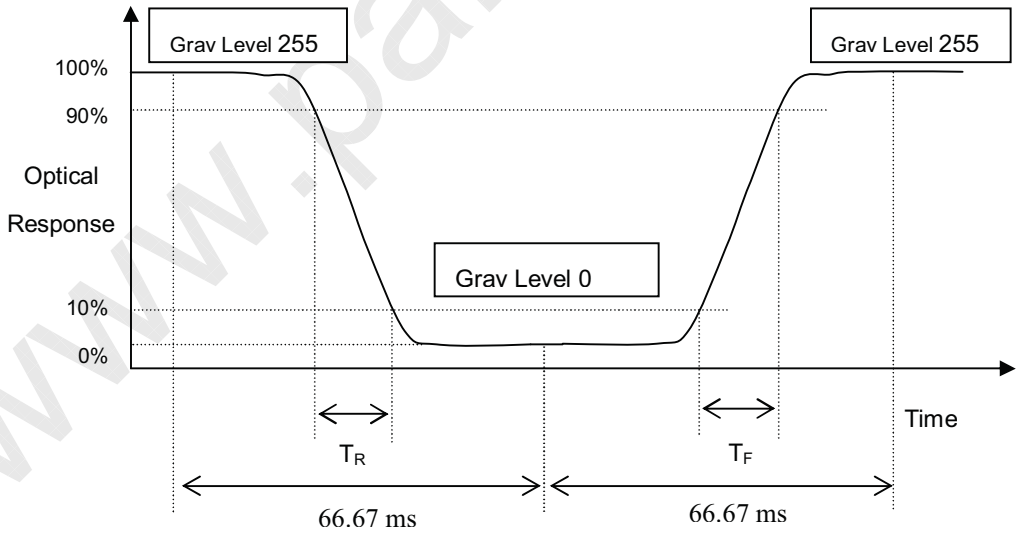
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

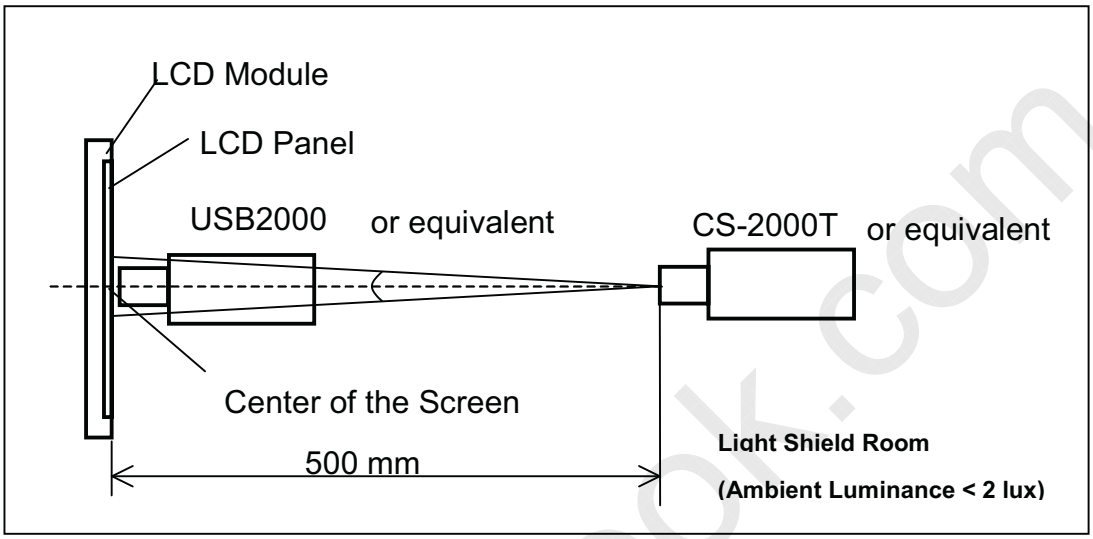
Measure the luminance of White at 5 points

L_{AVE} = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

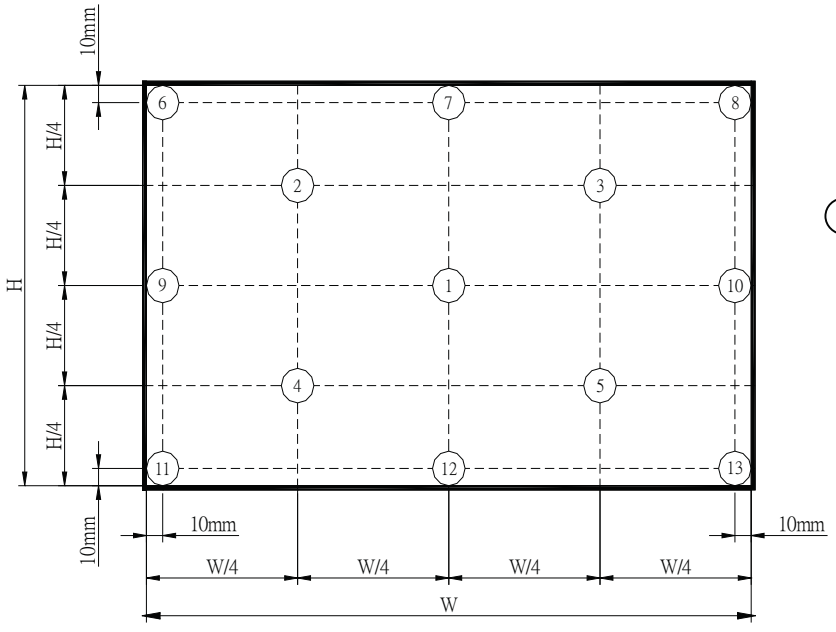


Note (6) Definition of White Variation (δW):

Measure the luminance of White at 5 points

δW_{5p} = {Maximum [L (1)~L (5)] / Minimum [L (1)~ L (5)]}*100%

δW_{13p} = {Maximum [L (1)~L (13)] / Minimum [L (1)~ L (13)]}*100%



X : Test Point

X=1 to 13

Active area

Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

Note (8) Definition of color gamut (C.G%):

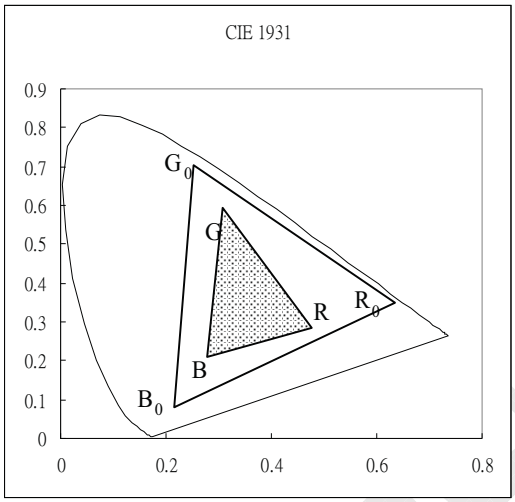
C.G%= Area (R, G, B) / Area (R_0, G_0, B_0,)* 100%

R_0, G_0, B_0: CIE1931 coordinates of red, green, and blue defined by NTSC.

R, G, B: CIE1931 coordinates of red, green, and blue in module at 63 gray level.

Area (R_0, G_0, B_0): Area of the triangle defined by coordinate R_0, G_0, B_0.

Area(R, G, B): Area of the triangle defined by coordinate R, G, B And just take the part that inside the Area(R_0, G_0, B_0), ignoring extension area.



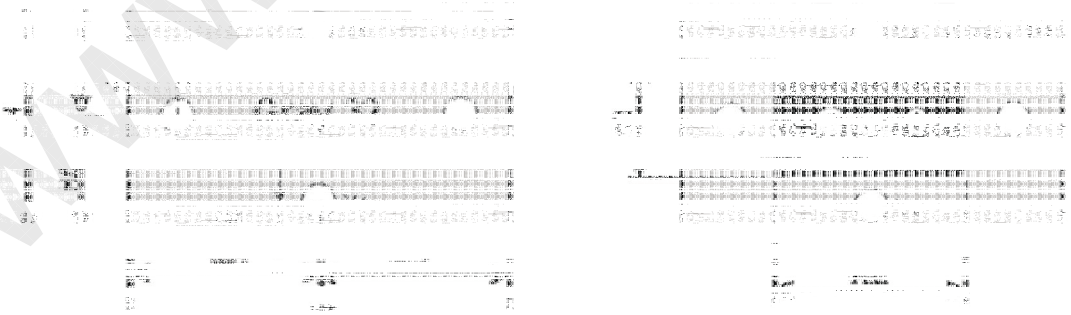
Note (9) Cross Talk (CT):

$CT = |Y_B - Y_A| / Y_A \times 100\%$

Where

Y_A=Luminance of measured location in left figure

Y_B=Luminance of measured location in right figure



6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	60ºC, 240 hours	(1) (2)
Low Temperature Storage Test	-20ºC, 240 hours	
Thermal Shock Storage Test	-20ºC, 0.5hour←→60℃, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	50ºC, 240 hours	
Low Temperature Operation Test	0ºC, 240 hours	
High Temperature & High Humidity Operation Test	50°C, 80% RH, 240 hours	
High Temperature & High Humidity Storage Test	40°C, 90% RH, 240 hours	
ESD Test (Operation)	150pF, 330Ω, 1sec/cycle Condition 1 : Contact Discharge, ±8KV Condition 2 : Air Discharge, ±15KV	(1)
Shock (Non-Operating)	220G, 2ms, half sine wave,1 time for each direction of ±X,±Y,±Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

Note (1) criteria : Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

7. PACKING

7.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

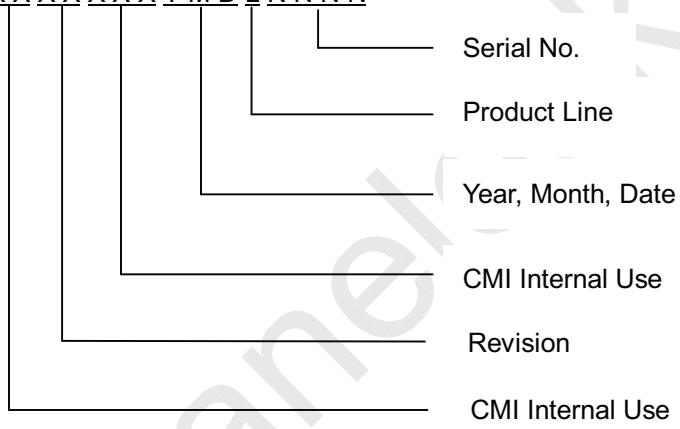
(The model name and revision shown at right side on the label is for customer recognition,

and the left side is for INX internal use.).

(a) Model Name: N156HCA-EAB

(b) Revision: Rev. XX, for example: C1, C2 …etc.

(c) Serial ID: X X X X X X Y M D L N N N N



(d) Production Location: MADE IN XXXX.

(e) UL/CB logo: XXXX is UL factory ID.

Serial ID includes the information as below:

(a) Manufactured Date: Year: 0~9, for 2020~2029

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

7.2 CARTON

(1)Box Dimensions : 500(L)*370(W)*270(H)
(2)20 Modules/Carton

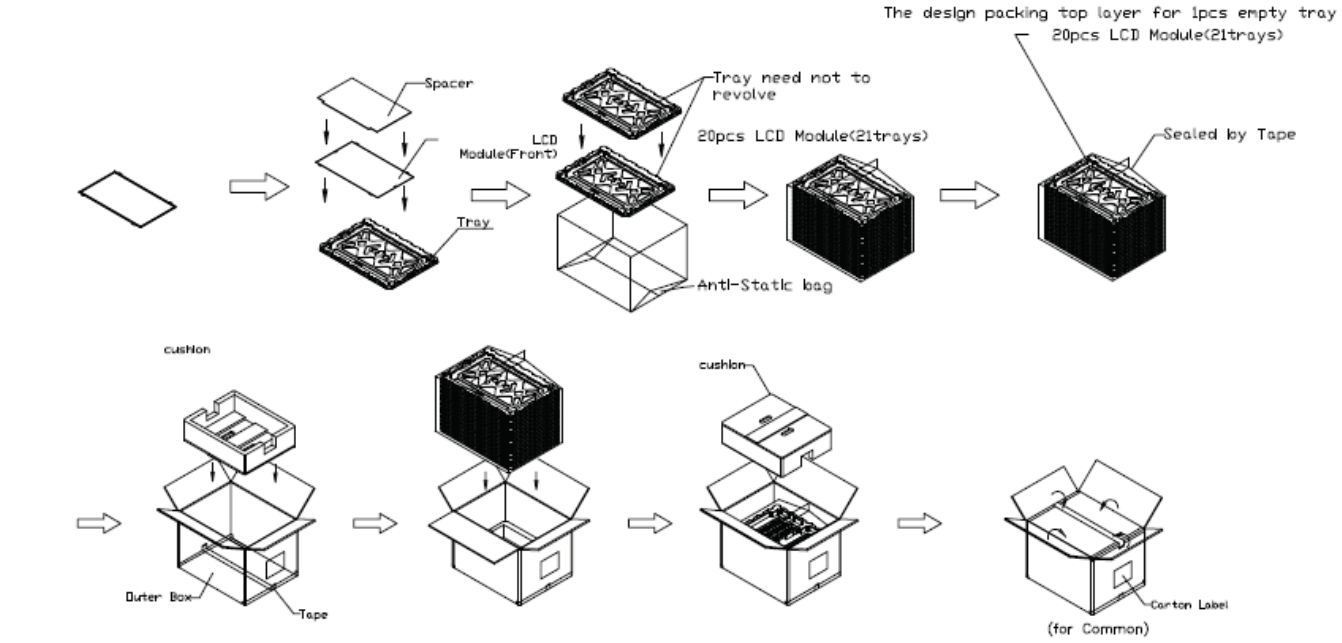


Figure. 7-2 Packing method

7.3 PALLET

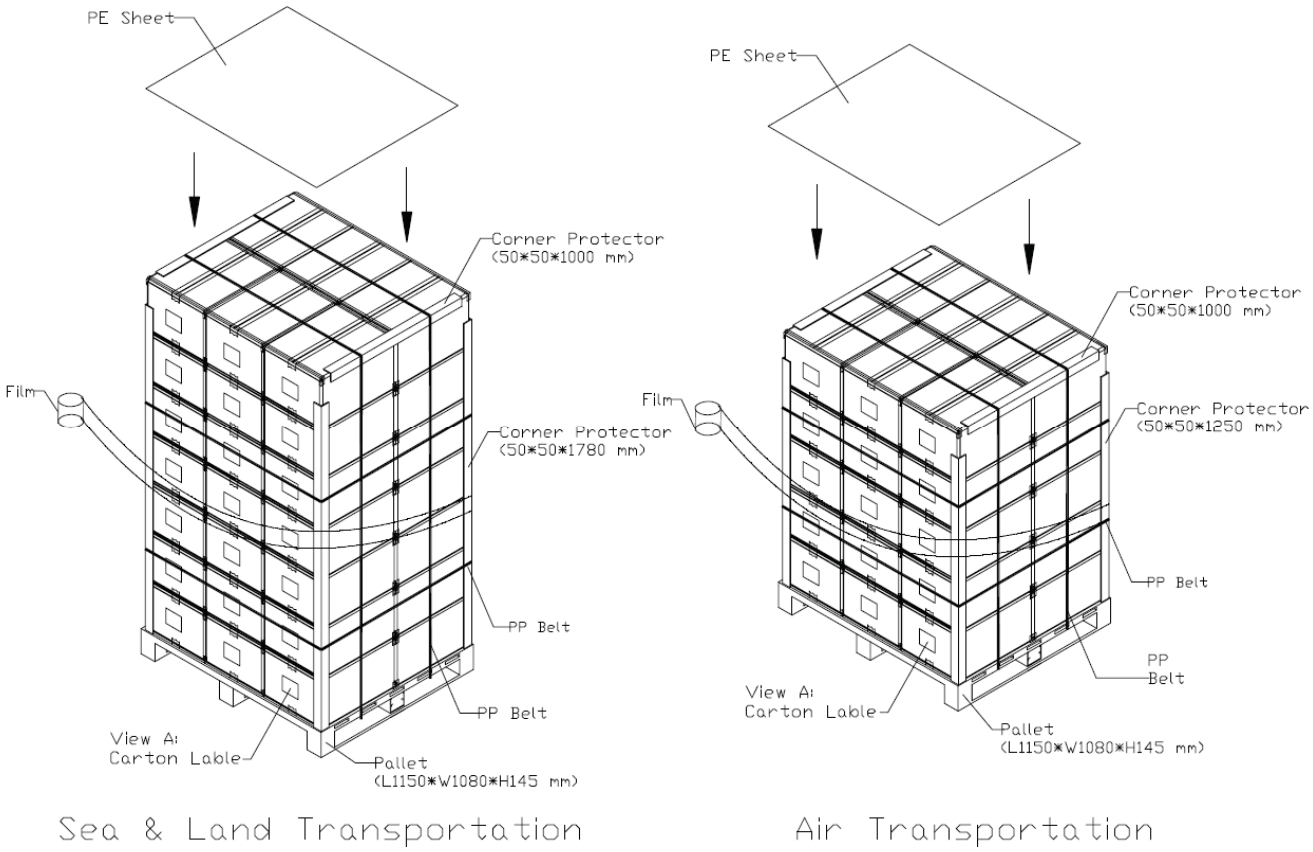
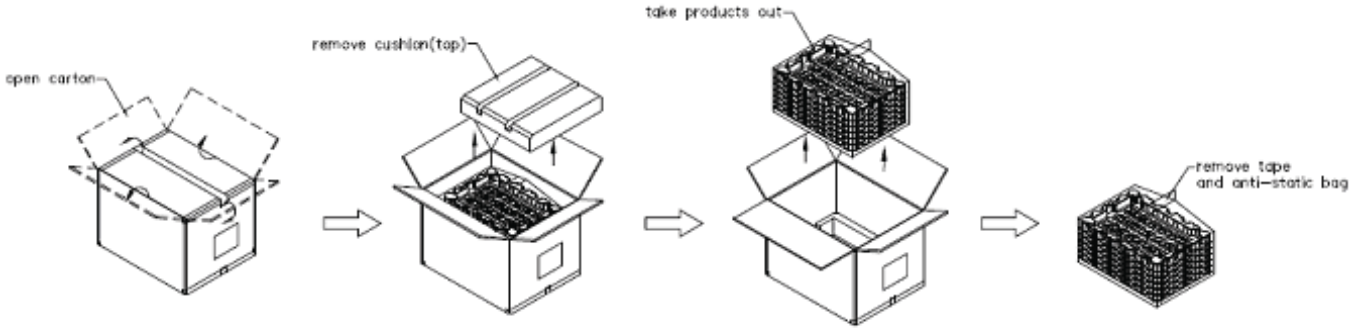
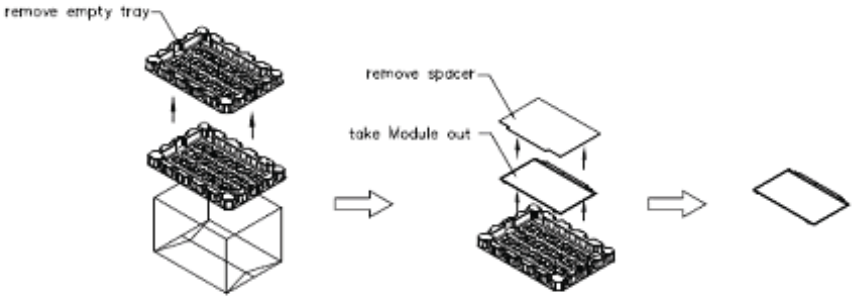


Figure. 7-3 Packing method

7.4 UN-PACKAGING METHOD





8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMIS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

Appendix. EDID DATA STRUCTURE

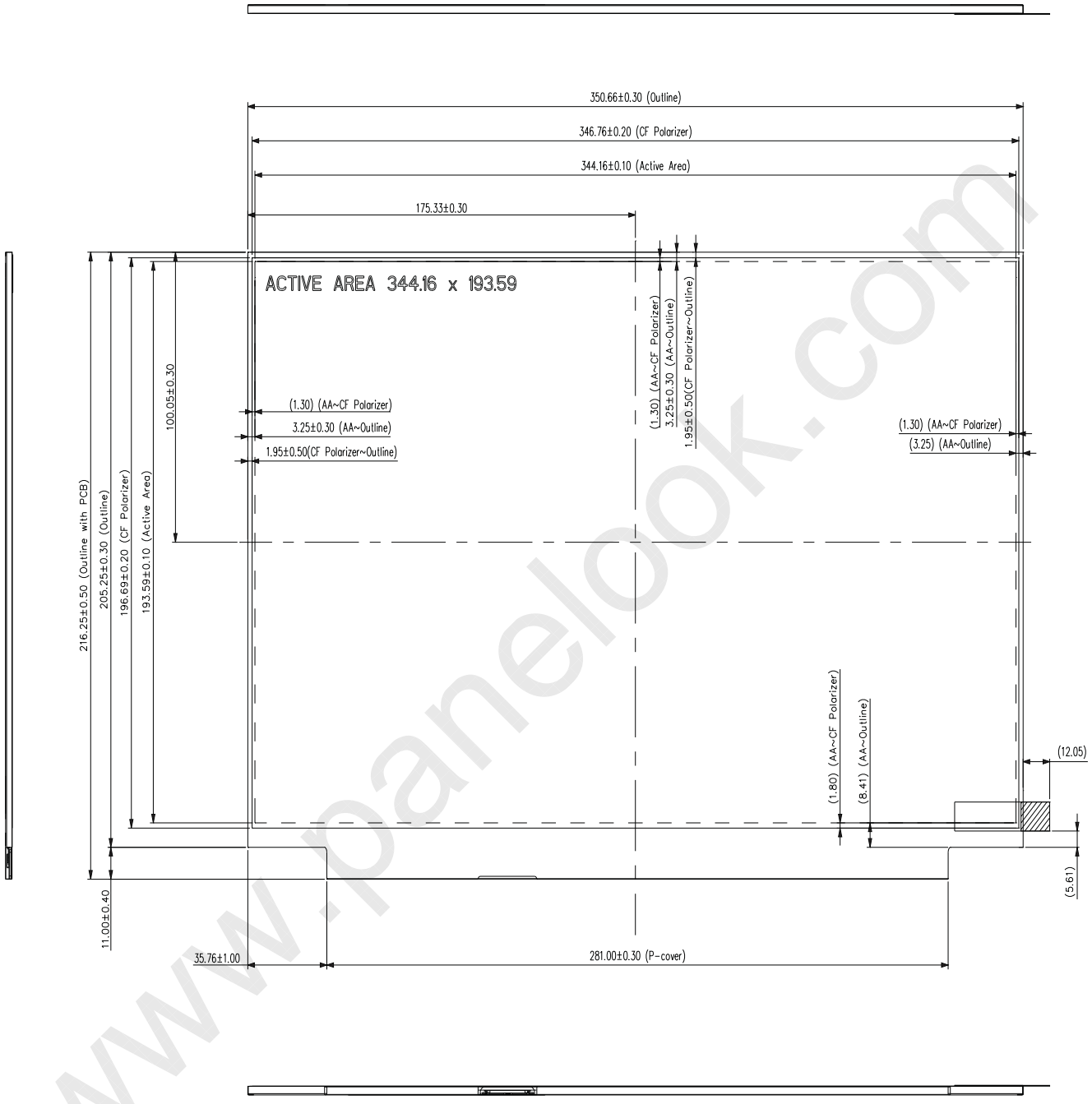
The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

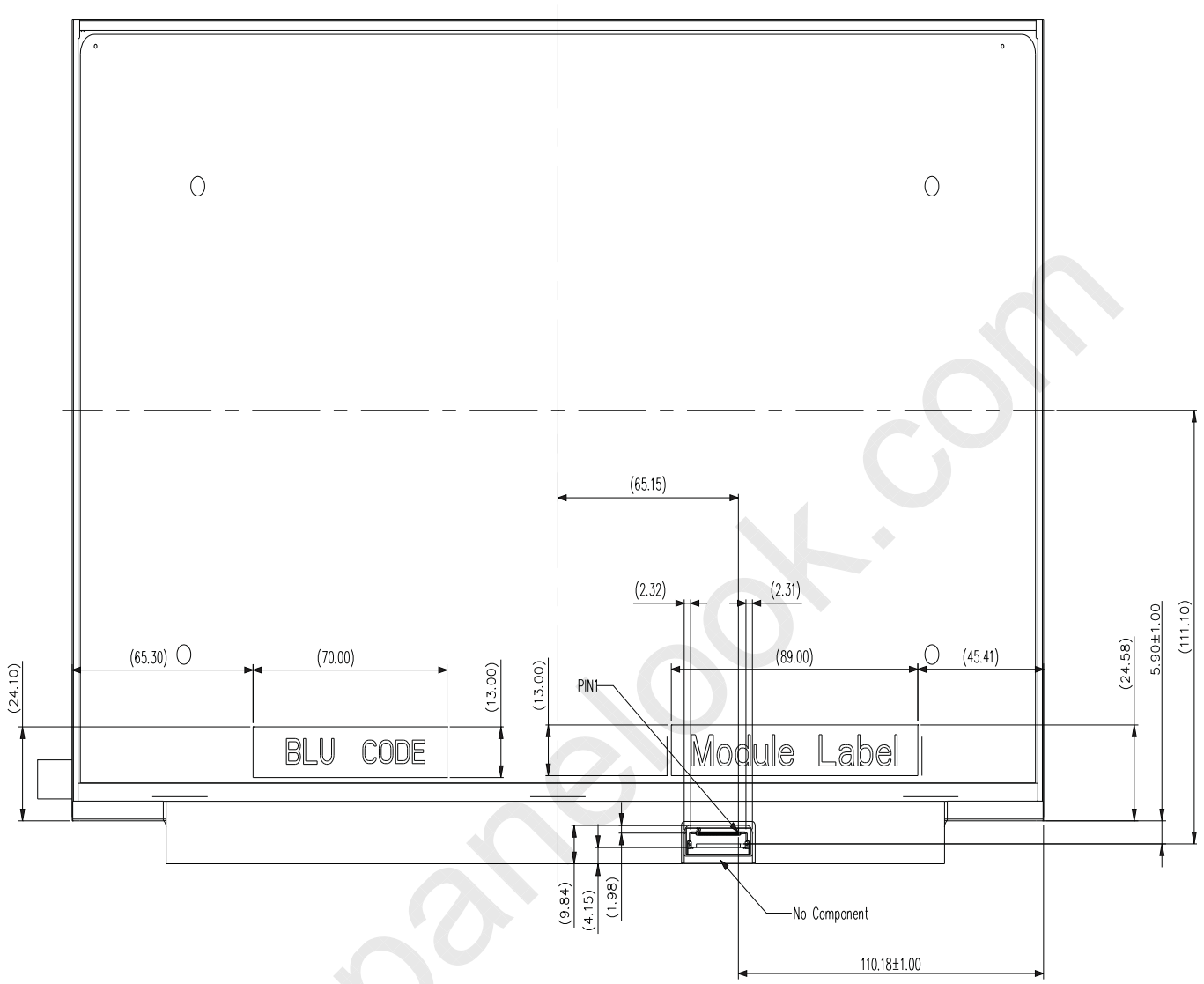
Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	00	Header	00	00000000
1	01	Header	FF	11111111
2	02	Header	FF	11111111
3	03	Header	FF	11111111
4	04	Header	FF	11111111
5	05	Header	FF	11111111
6	06	Header	FF	11111111
7	07	Header	00	00000000
8	08	EISA ID manufacturer name ("CMN")	0D	00001101
9	09	EISA ID manufacturer name	AE	10101110
10	0A	ID product code (LSB)	E7	11100111
11	0B	ID product code (MSB)	15	00010101
12	0C	ID S/N (fixed "0")	00	00000000
13	0D	ID S/N (fixed "0")	00	00000000
14	0E	ID S/N (fixed "0")	00	00000000
15	0F	ID S/N (fixed "0")	00	00000000
16	10	Week of manufacture (fixed week code)	2A	00101010
17	11	Year of manufacture (fixed year code)	1E	00011110
18	12	EDID structure version ("1")	01	00000001
19	13	EDID revision ("4")	04	00000100
20	14	Video I/P definition ("Digital")	A5	10100101
21	15	Active area horizontal (“34.416cm“)	22	00100010
22	16	Active area vertical (“19.359cm“)	13	00010011
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support ("RGB, Non-continous")	02	00000010
25	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	28	00101000
26	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	65	01100101
27	1B	Rx=0.59	97	10010111
28	1C	Ry=0.35	59	01011001
29	1D	Gx=0.33	54	01010100
30	1E	Gy=0.555	8E	10001110
31	1F	Bx=0.153	27	00100111
32	20	By=0.119	1E	00011110
33	21	Wx=0.313	50	01010000
34	22	Wy=0.329	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Manufacturer's reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001

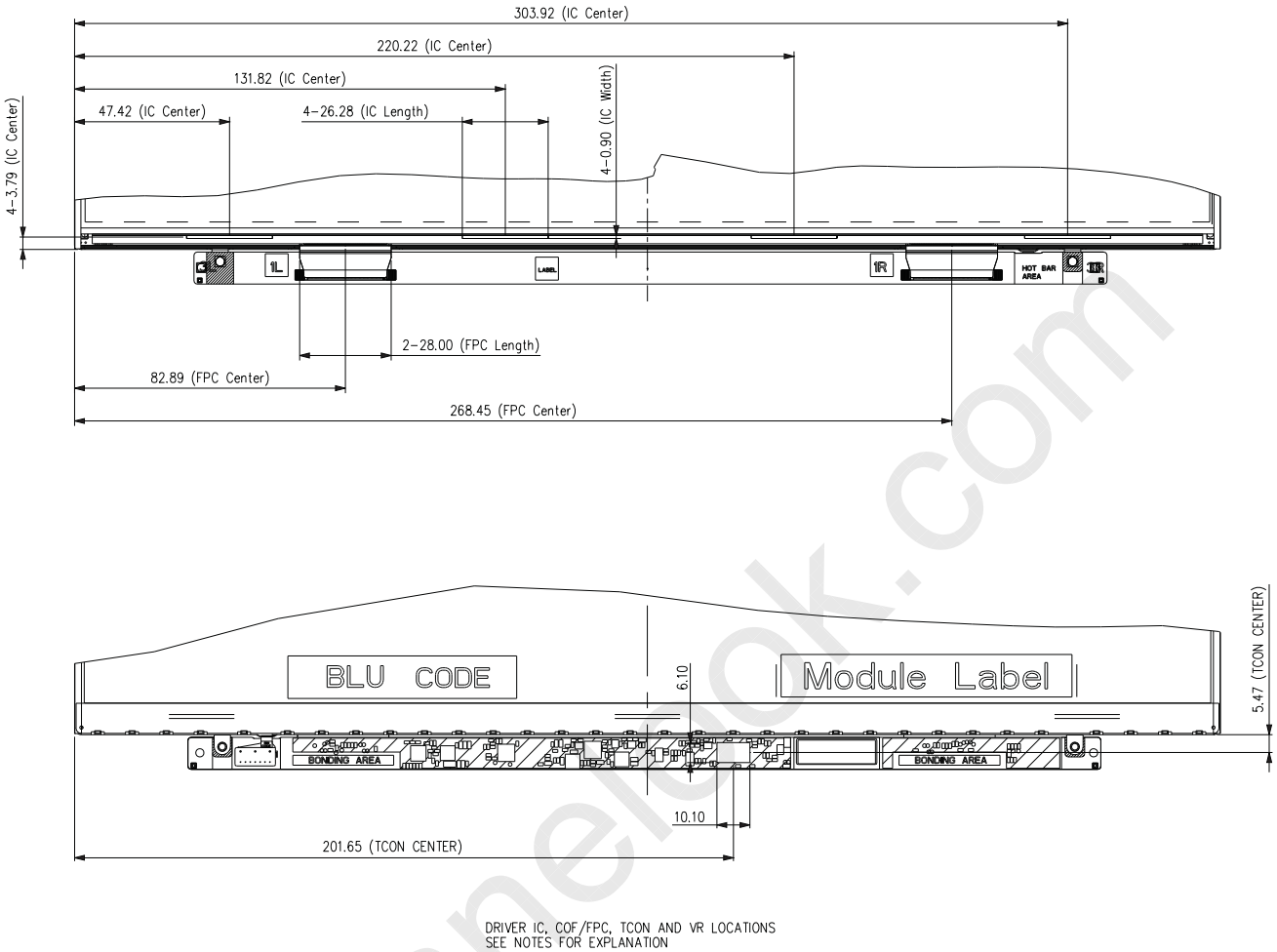
Byte # (decimal)				
	2A	Standard timing ID # 3	01	00000001
42	2B	Standard timing ID # 3	01	00000001
43	2C	Standard timing ID # 4	01	00000001
44	2D	Standard timing ID # 4	01	00000001
45	2E	Standard timing ID # 5	01	00000001
46	2F	Standard timing ID # 5	01	00000001
47	30	Standard timing ID # 6	01	00000001
48	31	Standard timing ID # 6	01	00000001
49	32	Standard timing ID # 7	01	00000001
50	33	Standard timing ID # 7	01	00000001
51	34	Standard timing ID # 8	01	00000001
52	35	Standard timing ID # 8	01	00000001
53	36	Detailed timing description # 1 Pixel clock ("152.84MHz")	B4	10110100
54	37	# 1 Pixel clock (hex LSB first)	3B	00111011
55	38	# 1 H active ("1920")	80	10000000
56	39	# 1 H blank ("330")	4A	01001010
57	3A	# 1 H active : H blank	71	01110001
58	3B	# 1 V active ("1080")	38	00111000
59	3C	# 1 V blank ("52")	34	00110100
60	3D	# 1 V active : V blank	40	01000000
61	3E	# 1 H sync offset (80")	50	01010000
62	3F	# 1 H sync pulse width ("54")	36	00110110
63	40	# 1 V sync offset : V sync pulse width ("6 : 8")	68	01101000
64	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width	00	00000000
65	42	# 1 H image size (“344 mm“)	58	01011000
66	43	# 1 V image size (“193 mm“)	C1	11000001
67	44	# 1 H image size : V image size	10	00010000
68	45	# 1 H boarder ("0")	00	00000000
69	46	# 1 V boarder ("0")	00	00000000
70	47	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	18	00011000
71	48	Detailed timing description # 2	00	00000000
72	49	# 2 Flag	00	00000000
73	4A	# 2 Reserved	00	00000000
74	4B	# 2 ASCII string Model name	FE	11111110
75	4C	# 2 Flag	00	00000000
76	4D	# 2 Character of Model name ("N")	4E	01001110
77	4E	# 2 Character of Model name ("1")	31	00110001
78	4F	# 2 Character of Model name ("5")	35	00110101
79	50	# 2 Character of Model name ("6")	36	00110110
80	51	# 2 Character of Model name ("H")	48	01001000
81	52	# 2 Character of Model name ("C")	43	01000011
82	53	# 2 Character of Model name ("A")	41	01000001
83	54	# 2 Character of Model name ("-")	2D	00101101
84	55	# 2 Character of Model name ("E")	45	01000101
85	56	# 2 Character of Model name ("A")	41	01000001

Byte #(decimal)				
	57	# 2 Character of Model name ("B")	42	01000010
86	58	# 2 New line character indicates end of ASCII string	0A	00001010
87	59	# 2 Padding with "Blank" character	20	00100000
88	5A	Detailed timing description # 3	00	00000000
89	5B	# 3 Flag	00	00000000
90	5C	# 3 Reserved	00	00000000
91	5D	# 3 ASCII string Vendor	FE	11111110
92	5E	# 3 Flag	00	00000000
93	5F	# 3 Character of string ("C")	43	01000011
94	60	# 3 Character of string ("M")	4D	01001101
95	61	# 3 Character of string ("N")	4E	01001110
96	62	# 3 New line character indicates end of ASCII string	0A	00001010
97	63	# 3 Padding with "Blank" character	20	00100000
98	64	# 3 Padding with "Blank" character	20	00100000
99	65	# 3 Padding with "Blank" character	20	00100000
100	66	# 3 Padding with "Blank" character	20	00100000
101	67	# 3 Padding with "Blank" character	20	00100000
102	68	# 3 Padding with "Blank" character	20	00100000
103	69	# 3 Padding with "Blank" character	20	00100000
104	6A	# 3 Padding with "Blank" character	20	00100000
105	6B	# 3 Padding with "Blank" character	20	00100000
106	6C	Detailed timing description # 4	00	00000000
107	6D	# 4 Flag	00	00000000
108	6E	# 4 Reserved	00	00000000
109	6F	# 4 ASCII string Model Name	FE	11111110
110	70	# 4 Flag	00	00000000
111	71	# 4 Character of Model name ("N")	4E	01001110
112	72	# 4 Character of Model name ("1")	31	00110001
113	73	# 4 Character of Model name ("5")	35	00110101
114	74	# 4 Character of Model name ("6")	36	00110110
115	75	# 4 Character of Model name ("H")	48	01001000
116	76	# 4 Character of Model name ("C")	43	01000011
117	77	# 4 Character of Model name ("A")	41	01000001
118	78	# 4 Character of Model name ("-")	2D	00101101
119	79	# 4 Character of Model name ("E")	45	01000101
120	7A	# 4 Character of Model name ("A")	41	01000001
121	7B	# 4 Character of Model name ("B")	42	01000010
122	7C	# 4 New line character indicates end of ASCII string	0A	00001010
123	7D	# 4 Padding with "Blank" character	20	00100000
124	7E	Extension flag	00	00000000
125	7F	Checksum	A5	10100101

Appendix. OUTLINE DRAWING







DRIVER IC, COF/FPC, TCON AND VR LOCATIONS
SEE NOTES FOR EXPLANATION

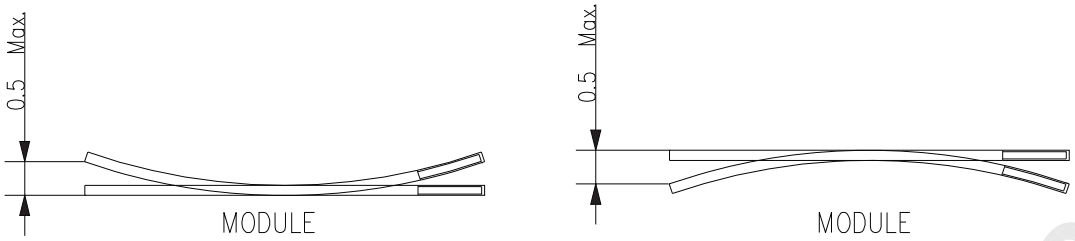


FIGURE 1

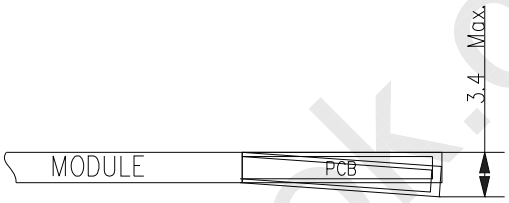


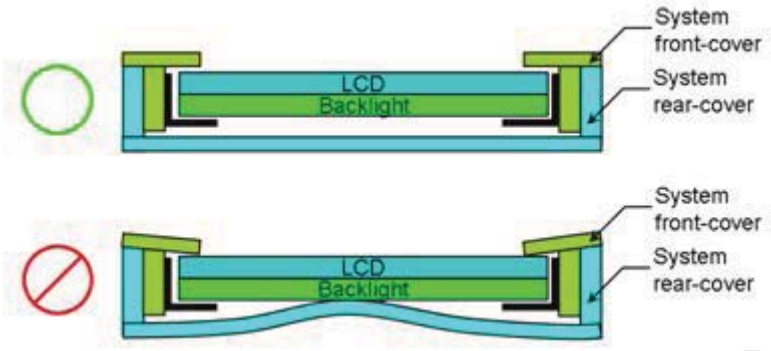
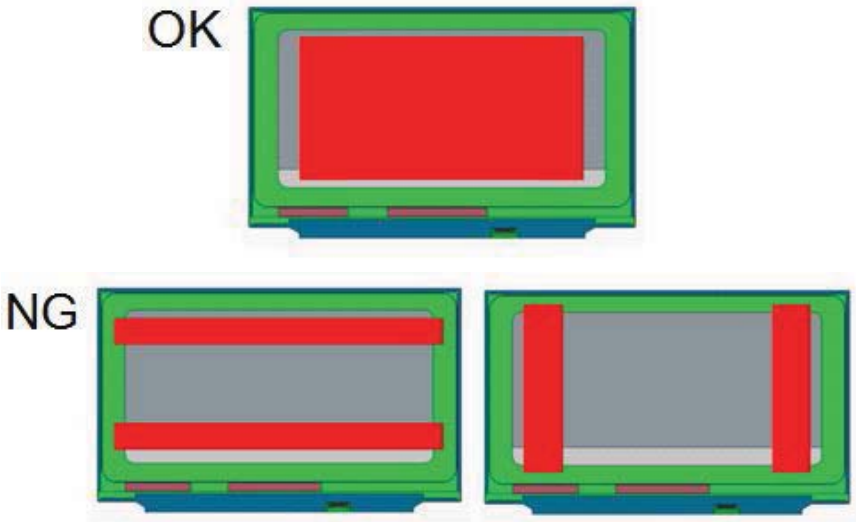
FIGURE 2

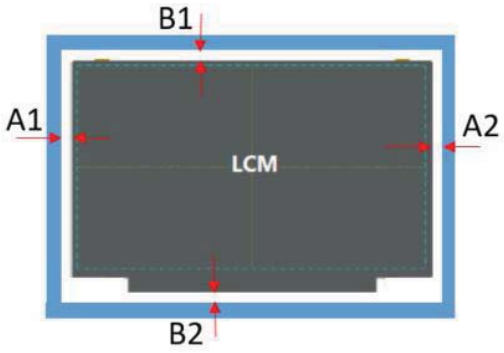
NOTES :
1. IN ORDER TO AVOID ABNORMAL DISPLAY, POOLING AND WHITE SPOT, NO OVERLAPPING IS SUGGESTED AT CABLES, ANTENNAS, CAMERA, WLAN, WAN OR FOREIGN OBJECTS OVER FPC/COF, T-CON AND VR LOCATIONS.
2. LVDS/EDP CONNECTOR IS MEASURED AT PIN1 AND ITS MATING LINE.
3-1. MODULE FLATNESS SPEC (0.5) mm MAX. (SEE FIGURE 1).
3-2. MODULE WITH PCB FLATNESS SPEC 3.4 MAX. (SEE FIGURE 2)
4. "( )" MARKS THE REFERENCE DIMENSION.
5. LCD HIGHEST PORTION MUST BE TOP POLARIZER AND OTHER LCM MATERIALS MUST BE LOWER THAN TOP POLARIZER. THE SOP SHOULD REFER TO "DN0566762" IN INX
6. MEASUREMENT OF THICKNESS MUST BE MEASURED BY CALIPER OR MICROMETER.

Note. Dimensions measuring instruments as below,

1. Length/ Width/Thickness : Caliper
2. Height : Height gauge

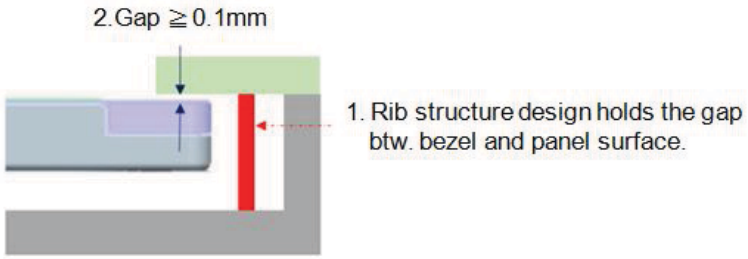
Appendix. SYSTEM COVER DESIGN GUIDANCE

0.	**Permanent deformation of system cover after reliability test**
	
Definition	System cover including front and rear cover may deform during reliability test. Permanent deformation of system front and rear cover after reliability test should not interfere with panel. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
1	**Sponge area design behind panel**
	
Definition	Sponge area design behind panel can not be across the panel metal rear and the reflector at the same time. It can be on the reflector area only.
2	**Gap between system rear-cover & panel**
	
Definition	The maximum thickness of sponge on the system rear-cover can not interfere to the maximum thickness of panel. Because the interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, and cell crack may occur. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
3	**Gap Design between panel & around structure**

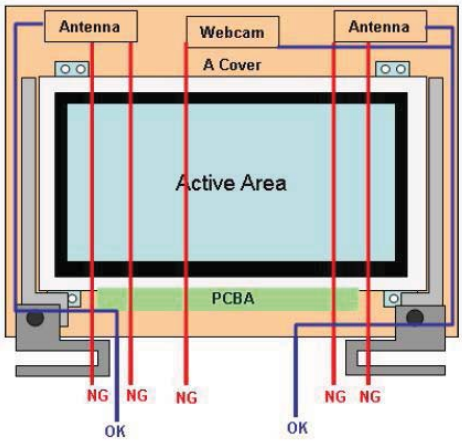


Item	Suggestion	Remark
A1	A1≧0.5	Gap≧ Panel outline max. tolerance + Assembly max. tolerance
A2	A2≧0.5	
B1	B1≧0.5	
B2	B2≧0.8	

Definition	Gap Design between panel & around structure needs to consider the maximum tolerances of panel outline and assembly at the same time. Gap Design suggestion is shown as A1/A2/B1/B2 on the chart.
4	**Gap between panel & bezel**

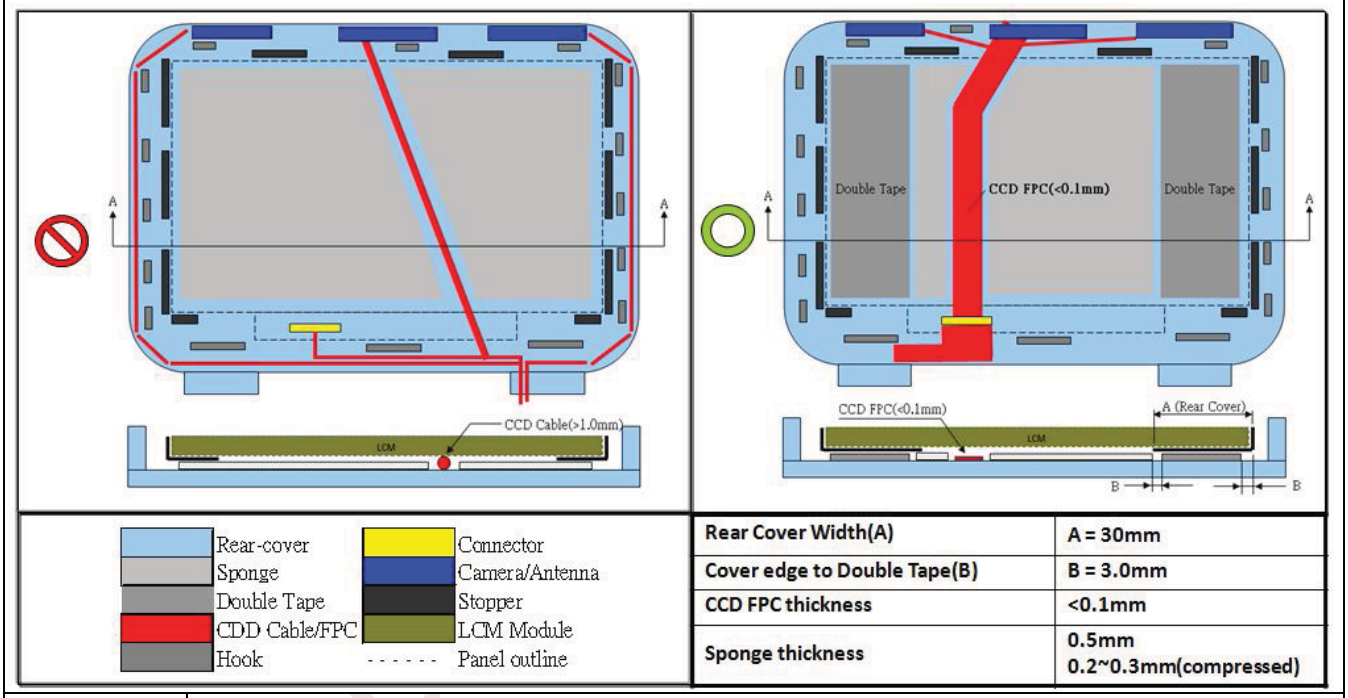


Definition	The gap between system bezel & panel surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system font-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test, or during pooling inspection procedure. To remain the sufficient gap, design with system rib higher than maximum panel thickness is recommended. The sufficient gap design is greater or equal to 0.1mm.
5	**Cable routing behind panel**



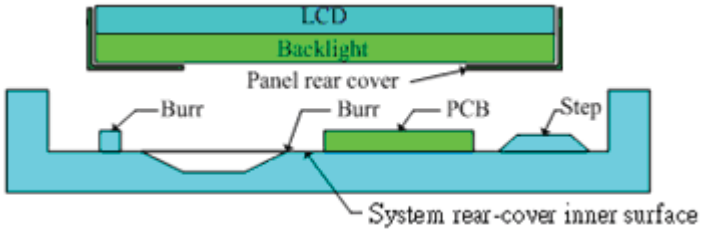
Definition	It is strongly recommended that cables route around the panel outline, not overlap with the panel outline (including PCB). Because issue such as abnormal display & white spot after backpack test, hinge test, twist test or pogo test may occur. If any routings across panel outline are needed, we suggest design as below: -Using FFC/FPC to replace cables. -Routing at the right or left area of panel metal rear. -Avoid any routings at the step of panel or A cover. -No interference to panel. -It should not overlap TCON, COF/FPC, Driver IC
6	**Interference examination of antenna cable and Web Cam wire**

- To prevent panel damage, we suggest using CCD FPC to replace CCD cable
- Using double tape to fix LCM module for no bracket design.

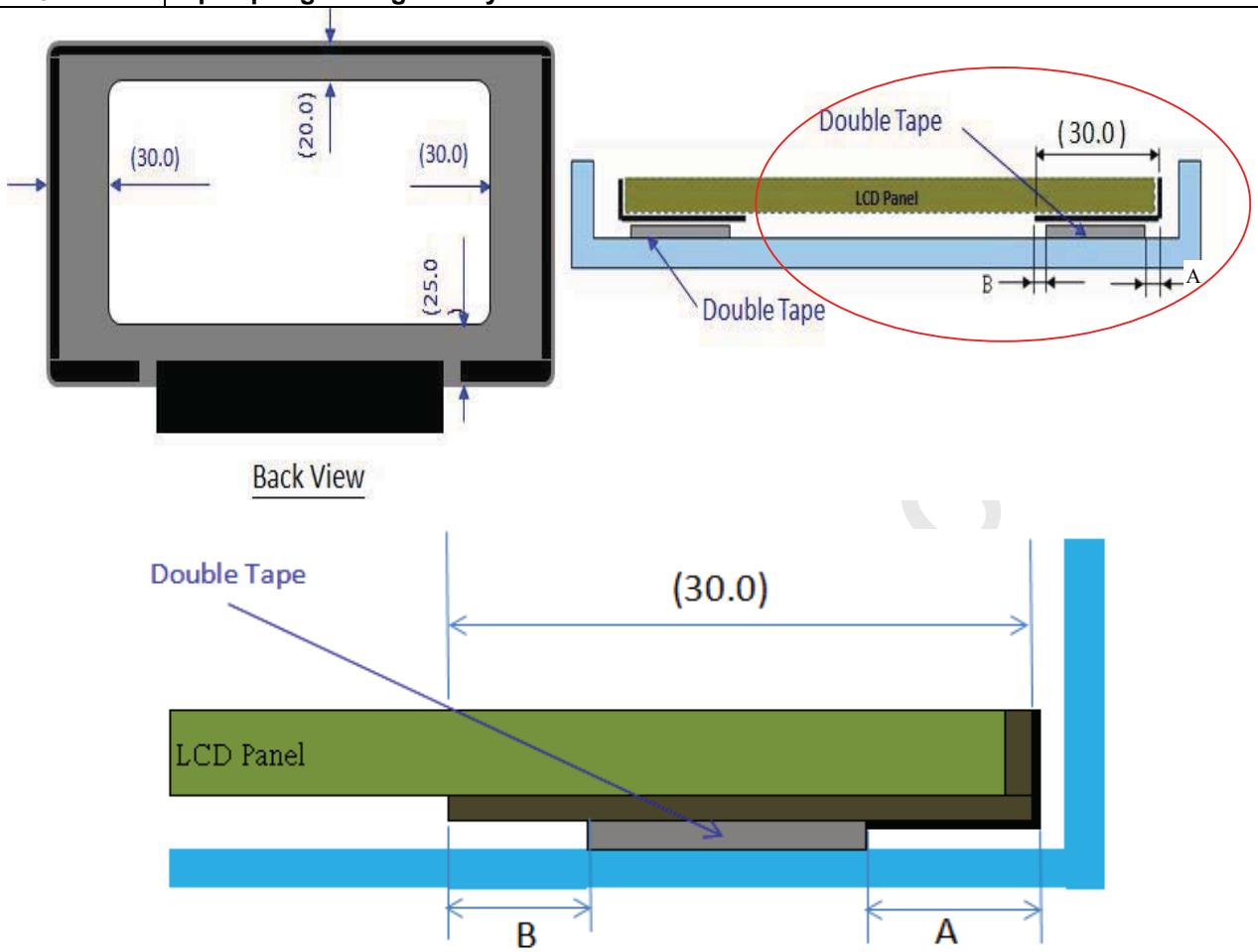
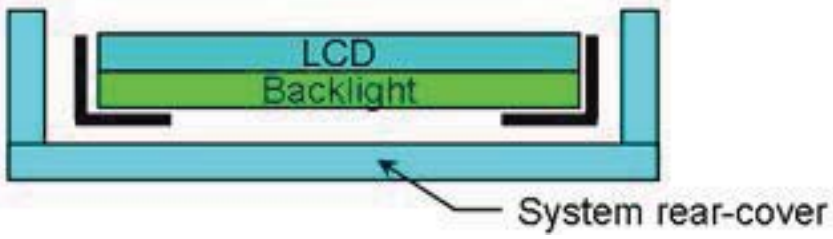


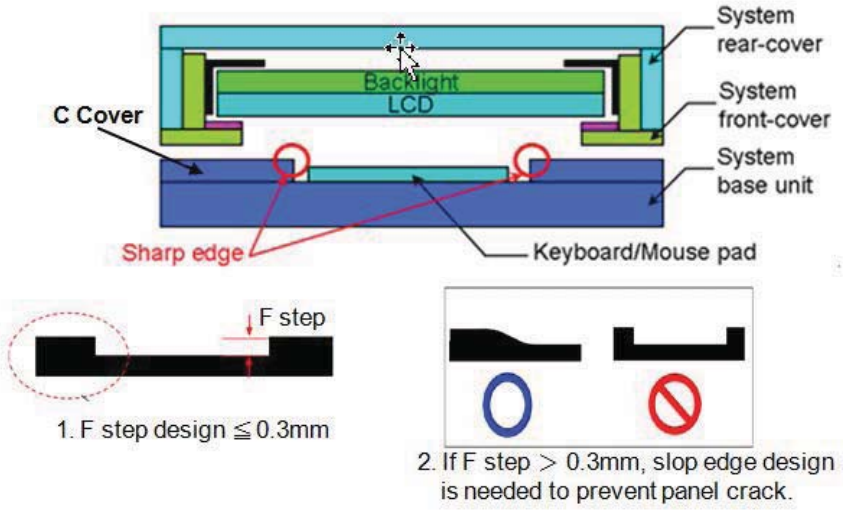
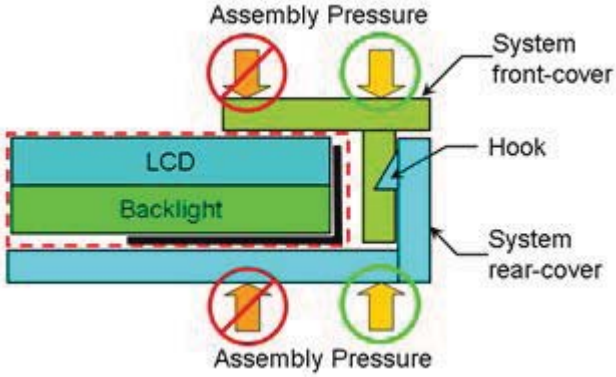
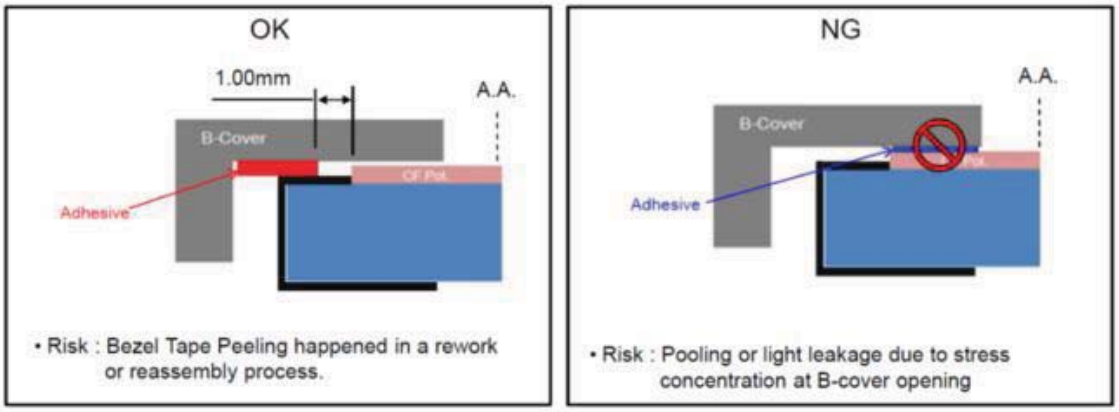
Rear Cover Width(A)	A = 30mm
Cover edge to Double Tape(B)	B = 3.0mm
CCD FPC thickness	<0.1mm
Sponge thickness	0.5mm 0.2~0.3mm(compressed)

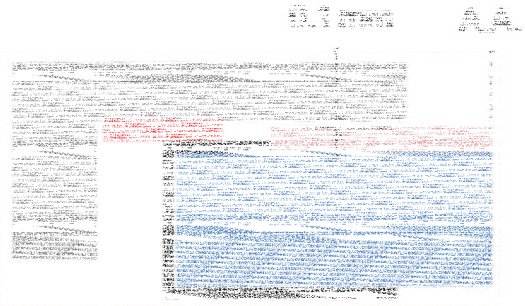
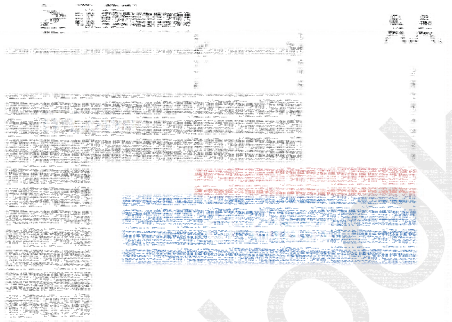
	If the antenna cable or Web Cam wire must overlap with the panel outline, both sides of the antenna cable or Web Cam wire must have a sponge(Sponge material can not contain NH3) and sponge require higher antenna cable or Web Cam wire.(Antenna cable or Web Cam wire should not overlap with TCON,COF/FPC,Driver IC) Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
7	**System rear-cover inner surface examination**

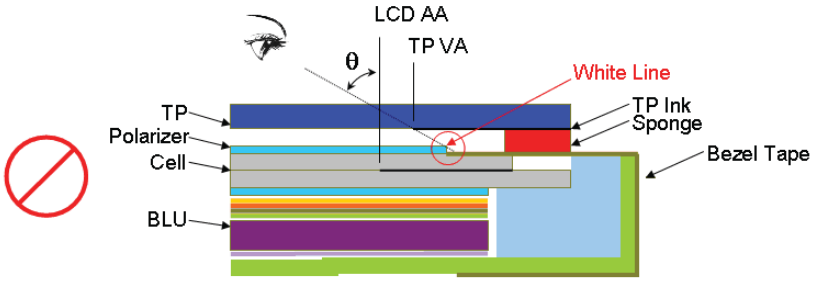


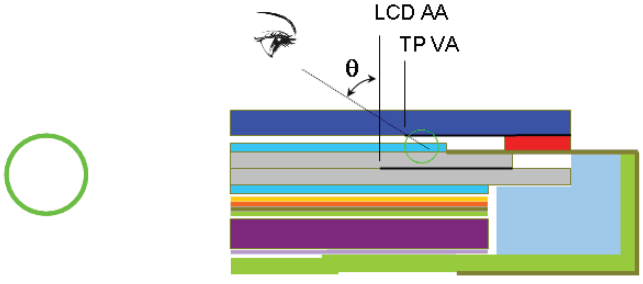
Definition	Burr at logo edge, steps, protrusions or PCB board may cause stress concentration. White spot or glass broken issue may occur during reliability test.

8	**Tape/sponge design on system inner surface**
	
Definition	To prevent peeling the bezel tape in rework process. The length of double tape is 30 – (A+B), A is bezel tape length and B is the double tape attaching tolerance. Ex :A :2mm, B:2mm, the length of double tape is 30-(2+2)=26mm.
9	**Material used for system rear-cover**
	 System rear-cover material: Al-Mg alloy System rear-cover thickness:1.5mm MIN
Definition	System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test, or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.

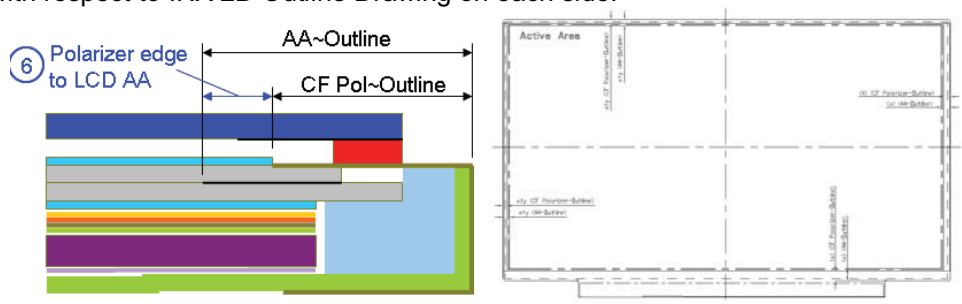
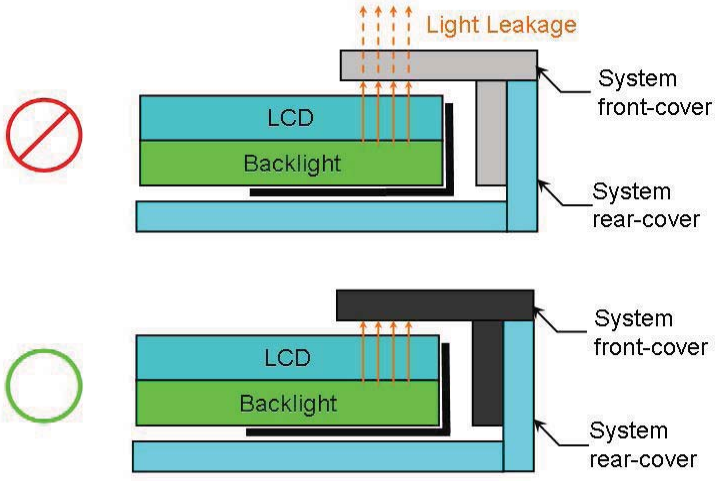
10	**C cover shape design**
	
Definition	The F step design on C Cover less than or equal to 0.3mm is recommended. If F step exceeds 0.3mm, the slop edge design is necessary to prevent panel crack.
11	**Assembly SOP examination for system front-cover with Hook design**
	
Definition	To prevent panel crack during system front-cover assembly process with hook design, it is not recommended to press panel or any location that related directly to the panel.
12	**Adhesive design between panel & bezel**
	
Definition	To prevent panel crack during system front-cover assembly process with double tape design, When system applied adhesive between B-Cover and LCD module, please design a distance 1.00mm between B-Cover's adhesive and CF pol. Do **NOT** put adhesive on CF pol. Adhesive material need be qualified to prevent from doing damage to cell tape after rework. Adhesive material need be qualified to prevent abnormal noise when hinge swinging test.

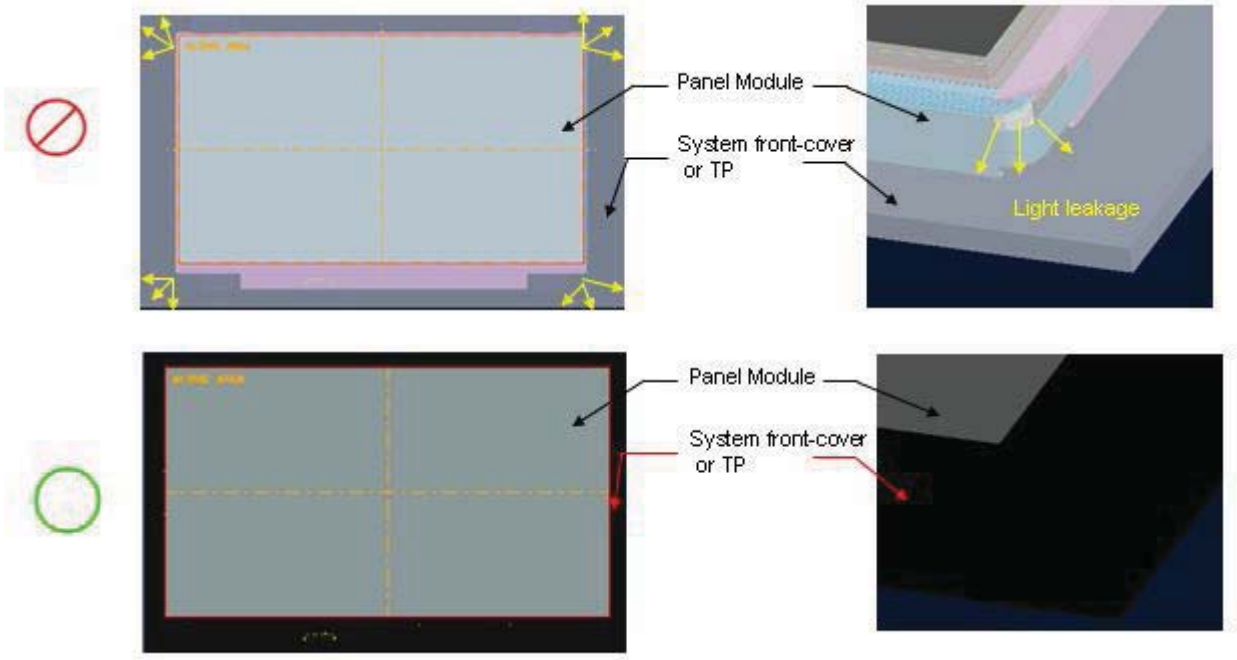
13	**System front-cover assembly reference with Double tape design**
	
Definition	To prevent system front-cover peeling at double tape contact area, A gap between B-Cover & CF-Pol. Is 0.1mm min.
14	System front-cover opening area reference with TFT-LCD module
	
Definition	To prevent panel the noise of B-cover & CF Pol. Distance from CF Pol. edge to front-cover edge more than 0.65mm.
15	**Touch Application : TP and LCD Module Combination for White Line Prevention**



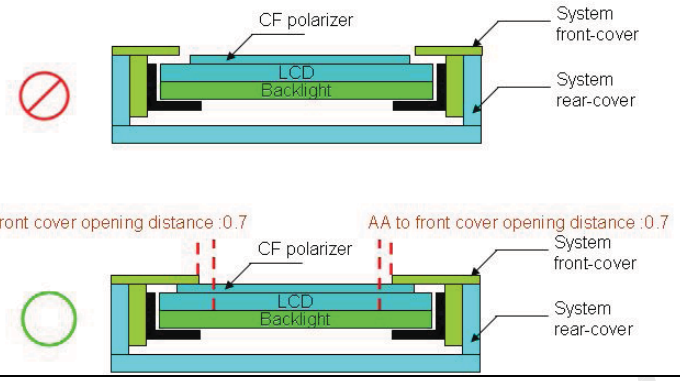
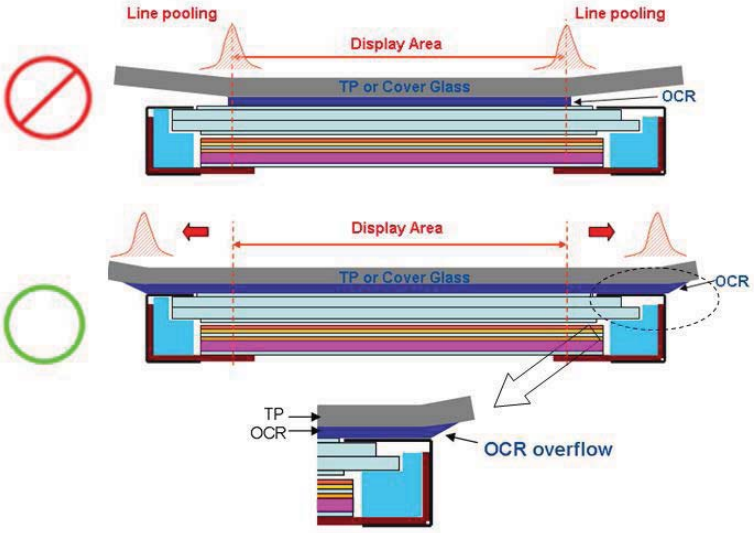
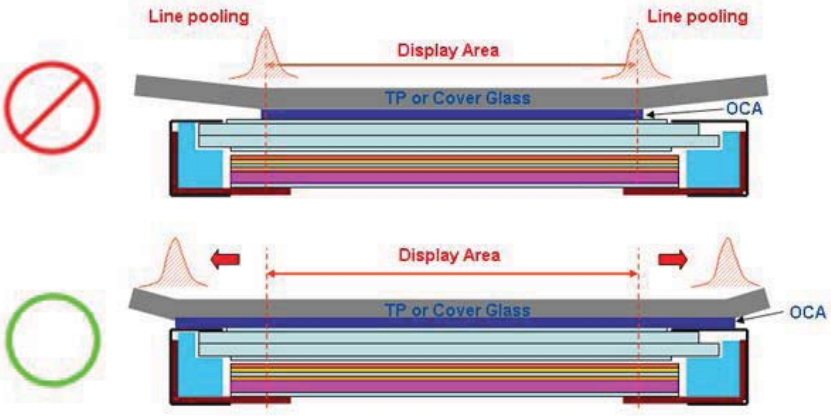


Parameter consideration for White Line Issue :	
1	TP VA to LCD AA distance
2	TP Assembly tolerance
3	TP Ink Printing tolerance
4	Sponge thickness and tolerance
5	Inspection/Viewing Angle specification
6	Polarizer edge to LCD AA distance and tolerance

	Polarizer edge to LCD AA distance can be derived by "AA~Outline" – "CF Pol~Outline" with respect to INX 2D Outline Drawing on each side. 
Definition	For using in Touch Application: to prevent White Line appears between TP and LCD module combination, the maximum inspection angle location must not fall onto LCD polarizer edge, otherwise light line near edge of polarizer will be appear. Parameters such as TP VA to LCD AA distance, TP assembly tolerance, TP Ink printing tolerance, Sponge thickness and tolerance, and Maximum Inspection/Viewing Angle, must be considered with respect to LCD module's Polarizer edge location and tolerance. This consideration must be taken at all four edges separately. The goal is to find parameters combination that allow maximum inspection angle falls inside polarizer black margin area. Note: Information for Polarizer edge location and its tolerance can be derived from INX 2D Outline Drawing ("AA ~Outline" - "CF Pol~Outline"). Note: Please feel free to contact INX FAE Engineer. By providing value of parameters above on each side, we can help to verify and pass the white line risk assessment for customer reference.
16	**Color of system front-cover material**
	



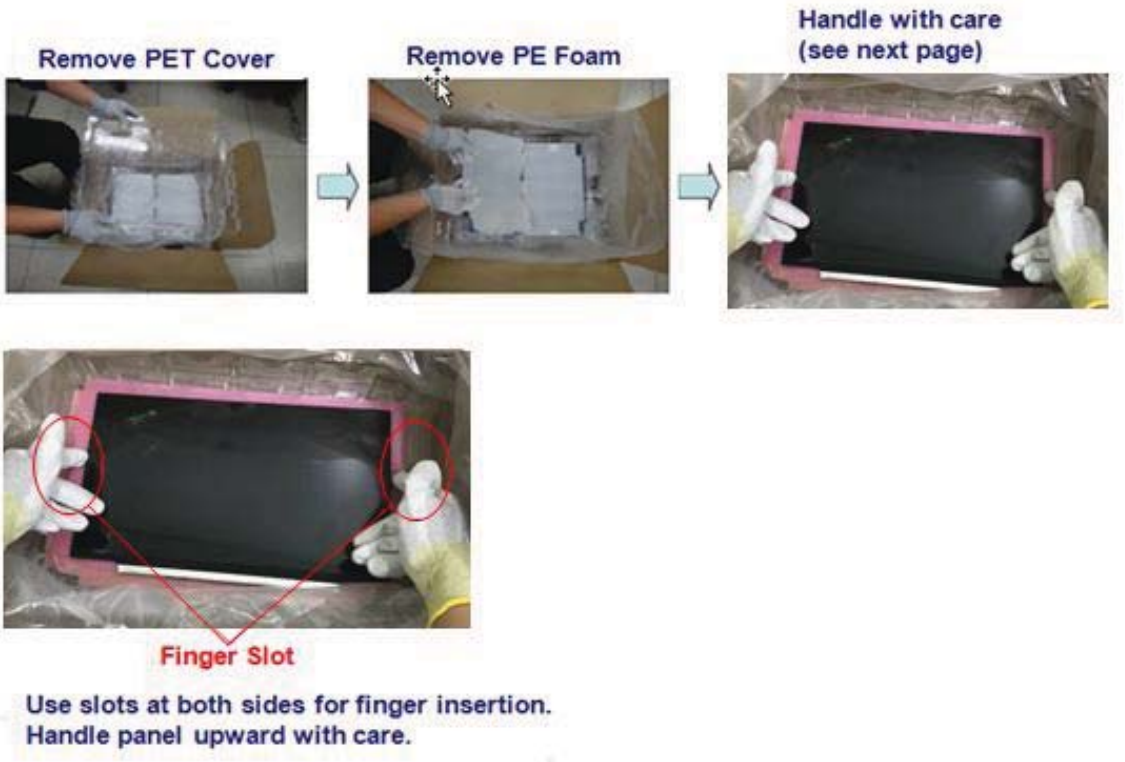
Definition	To prevent light leakage is seen at system front-cover due to material transparency, we suggest using dark color material (black) for system front-cover design.

17	**AA to front cover opening distance**
	
Definition	To prevent CF polarizer edge leakage .We suggest front cover opening no more than 0.7mm larger than active area on all 4 sides.
18	**Use OCR Lamination**
	
Definition	OCR glue as possible beyond module, in order to avoid Line Pooling
19	**Use OCA Lamination**
	
Definition	OCA glue as possible plastered throughout the module, in order to avoid Line Pooling.

Appendix. LCD MODULE HANDLING MANUAL

Purpose	• **This SOP is prepared to prevent panel dysfunction possibility through incorrect handling procedure.** • **This manual provides guide in unpacking and handling steps.** • **Any person which may contact / related with panel, should follow guide stated in this manual to prevent panel loss.**
1.	**Unpacking**

2.	**Panel Lifting**



3.	Do and Don't

Do :

- Handle with both hands.
- Handle panel at left and right edge.

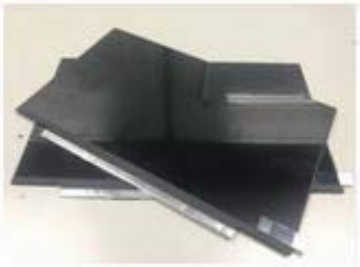
Don't :

- Lifting with one hand.

- Handle at PCBA side.

Don't :

- Stack panels.



- Press panel.

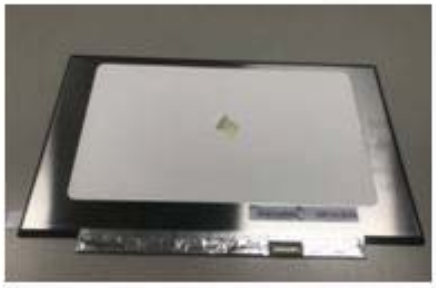
Don't :

- Put foreign stuff onto panel

- Put foreign stuff under panel

Don't :

- Paste any material unto white reflector sheet



Don't :

- Pull / Push white reflector sheet

Don't :

- Hold at panel corner.

Don't :

- Twist panel.

Do :

- Hold panel at top edge while inserting connector.

Don't :

- Press white reflector sheet while inserting connector.

Do :

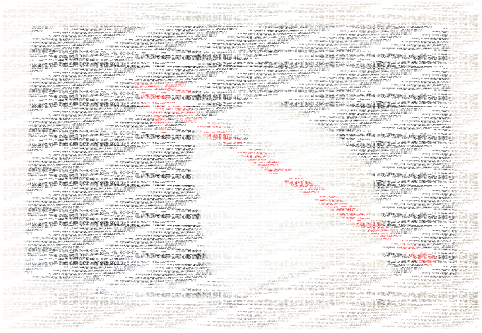
- Remove panel protector film starts from pull tape

Don't :

- Remove panel protector film From film another side.

Do:

- Remove panel protector film starts from lower right corner to top left



Don't:

- Remove panel protector Film parallel x-direction

Don't :

- Touch or Press PCBA Area.