INNOLUX 群創光電

PRODUCT SPECIFICATION

Doc. Number:

☐ Tentative Specification
☐ Preliminary Specification
■ Approval Specification

MODEL NO.: N080ICE
SUFFIX: GB1 (C2)

Customer:

APPROVED BY **SIGNATURE**

Name / Title _____ _____

Note :

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By

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REVISION HISTORY

Version	Date	Page	Description
0.0	Sep, 12, 2013	All	Spec Ver.0.0 was first issued.
1.0	Oct, 25, 2013	26~37	Add Packing ,System cover design guidance
2.0	Nov, 04, 2013	31~34	Update 2D drawing
3.0	Nov, 13, 2013	25	Update Image sticking spec.
4.0	Nov, 18, 2013	19~20	Update Power Sequence.
5.0	Dec, 03, 2013	4,25	Update Module size V ,Delete Image sticking spec.
6.0	Dec, 18, 2013	31~33 38~43	Update OUTLINE DRAWING Add NT35521 REGISTER SETTING

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N080ICE-GB1 is a 8" (8" diagonal) TFT Liquid Crystal Display module with LED Backlight unit and **31 pins MIPI** interface. This module supports 800 x 1280 WXGA mode.

1.2 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Screen Size	8" diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	800 x R.G.B. x 1280	pixel	-
Pixel Pitch	0.13455 (H) x 0.13455 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16,777,216 (8bit color depth)	color	-
Transmissive Mode	Normally black	-	-
Surface Treatment	Hard coating(3H), Low-Reflection	-	-
Luminance, White	350	Cd/m2	
Power Consumption	***Total 1.5 W (Max.) (panel 0.3 W (Max.), BL 1.2W (Max.))***		(1)

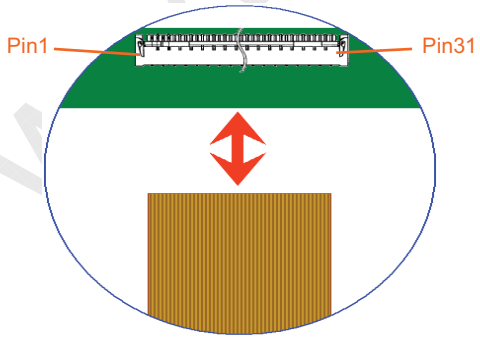
Note(1) The specified power consumption (with converter efficiency) is under the conditions at **VCI = 3.3 V, VDDI= 1.8V, fv = 60 Hz, Brightness = 350nits, I_{F_LED} = 20mA** and Ta = 25 ± 2 ºC, whereas **white** pattern is displayed.

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	120.15	120.65	121.15	mm	(1)
	Vertical (V)	187.14	187.64	188.14	mm	
	Thickness (T)			2.9 (w/o PCBA) 5.1 (w/ PCBA)	mm	
CF Polarizer	Horizontal	109.54	110.04	110.54	mm	
	Vertical	174.12	174.62	175.12	mm	
Active Area	Horizontal		107.64		mm	
	Vertical		172.224		mm	
Weight		-	-	99	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2.1 CONNECTOR TYPE



Please refer Appendix Outline Drawing for detail design.

Connector Part No.: **Panasonic AYF333135**

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

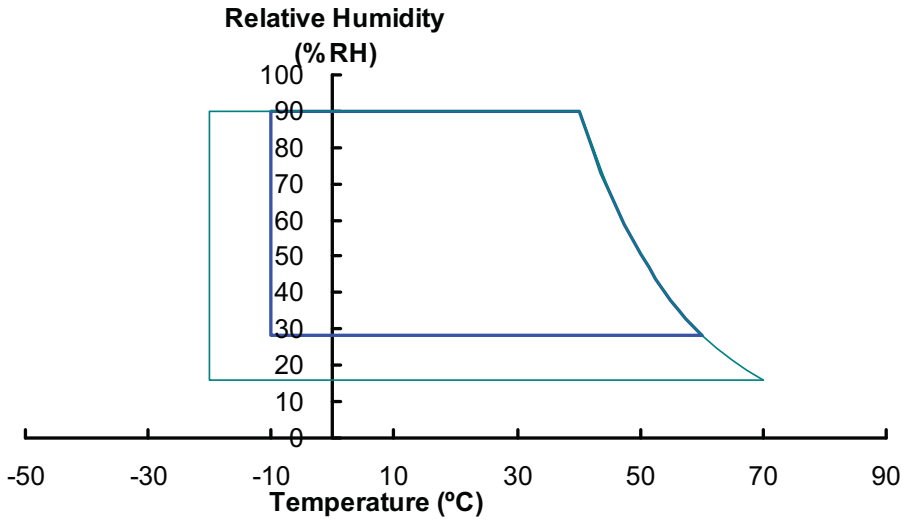
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+70	ºC	(1)
Operating Ambient Temperature	T_{OP}	-10	+60	ºC	(1), (2)

Note(1) (a) 90 %RH Max. (Ta <= 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note(2) The temperature of panel surface should be -10 ºC min. and 70 ºC max.



3.2 ELECTRICAL ABSOLUTE RATINGS

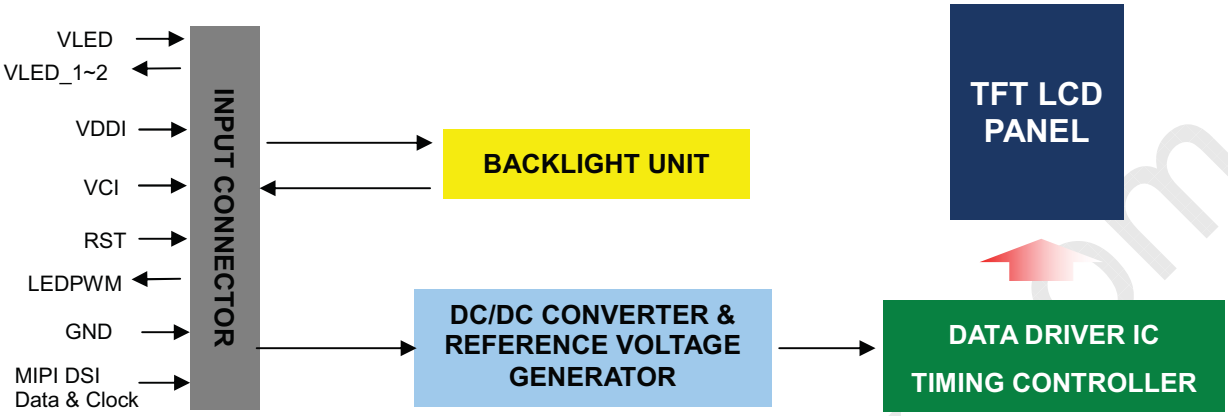
3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	**VCI**	**-0.3**	**+5.0**	**V**	(1)
	VDDI	**-0.3**	**+2.0**	**V**	(1)

Note(1) Stresses beyond those listed in above “ELECTRICAL ABSOLUTE RATINGS” may cause permanent damage to the device. Normal operation should be restricted to the conditions described in “ELECTRICAL CHARACTERISTICS”.

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



4.2. INTERFACE CONNECTIONS

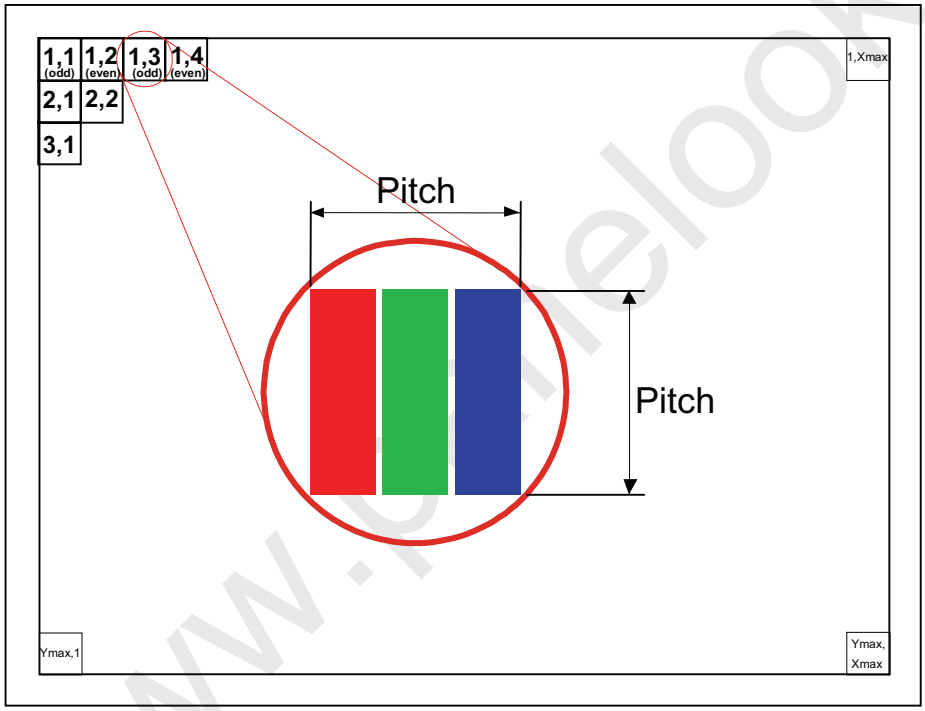
PIN ASSIGNMENT

Pin	Symbol	I/O	Description	Remark
1	GND	P	Ground	
2	GND	P	Ground	
3	GND	P	Ground	
4	D_0N	I	MIPI differential data0 input (Negative)	
5	RST	I	Device reset signal	
6	D0_P	I	MIPI differential data0 input (Positive)	
7	VCI	P	3.3V input	
8	GND	P	Ground	
9	VCI	P	3.3V input	
10	D1_N	I	MIPI differential data1 input (Negative)	
11	NC(MTP)	P	No connection, please keep it floating	
12	D1_P	I	MIPI differential data1 input (Positive)	
13	VDDI	P	1.8V input	
14	GND	P	Ground	
15	VDDI	P	1.8V input	
16	CLK_N	I	MIPI differential clock input (Negative)	
17	LEDPWM	O	PWM control signal for LED driver (CABC)	
18	CLK_P	I	MIPI differential clock input (Positive)	
19	VLED	P	Anode for light bar	
20	GND	P	Ground	
21	VLED	P	Anode for light bar	

22	D2_N	I	MIPI differential data2 input (Negative)	
23	ID		Ground	
24	D2_P	I	MIPI differential data2 input (Positive)	
25	LED1	P	Cathode for light bar	
26	GND	P	Ground	
27	LED2	P	Cathode for light bar	
28	D3_N	I	MIPI differential data3 input (Negative)	
29	GND	P	Ground	
30	D3_P	I	MIPI differential data3 input (Positive)	
31	GND	P	Ground	

Note (1) The first pixel is odd as shown in the following figure.

Note (2) Normal operation/BIST pattern selection. (Control by MIPI LP Command)



4.3 ELECTRICAL CHARACTERISTICS

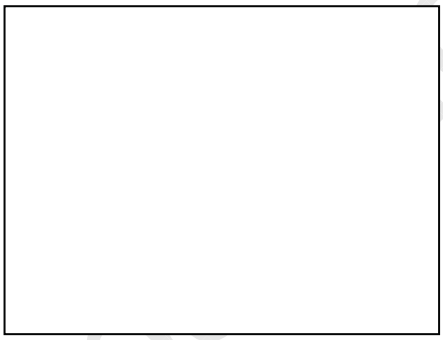
4.3.1 LCD ELETRONICS SPECIFICATION

Item		Symbol	Values			Unit	Remark
			Min.	Typ.	Max.		
Power supply voltage		VCI	3.0	3.3	3.6	V	
		VDDI	1.7	1.8	1.9	V	
VDDI High level input voltage		V_{IH2}	0.7 VDDI	-	VDDI	V	For I/O circuit
VDDI Low level input voltage		V_{IL2}	0	-	0.3 VDDI	V	
Power Supply Current	White	I_{VCI}	-	50	60	mA	Note (2)
		I_{VDDI}	-	45	55	mA	
Power Consumption		PLCD	-	-	300	mW	Note (3)

Note(1) The ambient temperature is Ta = 25 ± 2 ºC.

Note(2) The specified power supply current is under the conditions at VCI = 3.3 V, VDDI = 1.8 V, Ta = 25 ± 2 ºC, DC Current and f_v = 60 Hz, whereas a power dissipation check White pattern below is displayed.

b. White Pattern



Active Area

Note(3) The power consumption is specified at the white pattern with the maximum current.

4.3.2 LED CONVERTER SPECIFICATION

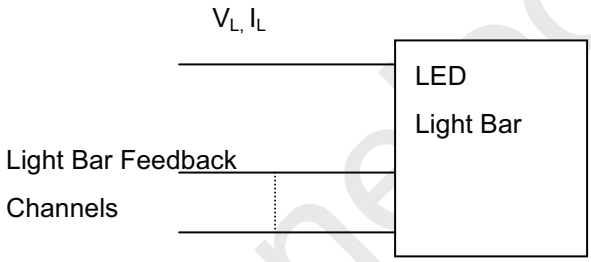
N/A

4.3.3 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V_L	8.4	9	9.6	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	I_L	-	120	-	mA	
Power Consumption	P_L	-	1.08	1.16	W	(3)
LED Life Time	L_{BL}	15000	-	-	Hrs	(4)

Note(1) LED current is measured by utilizing a high frequency current meter as shown below :

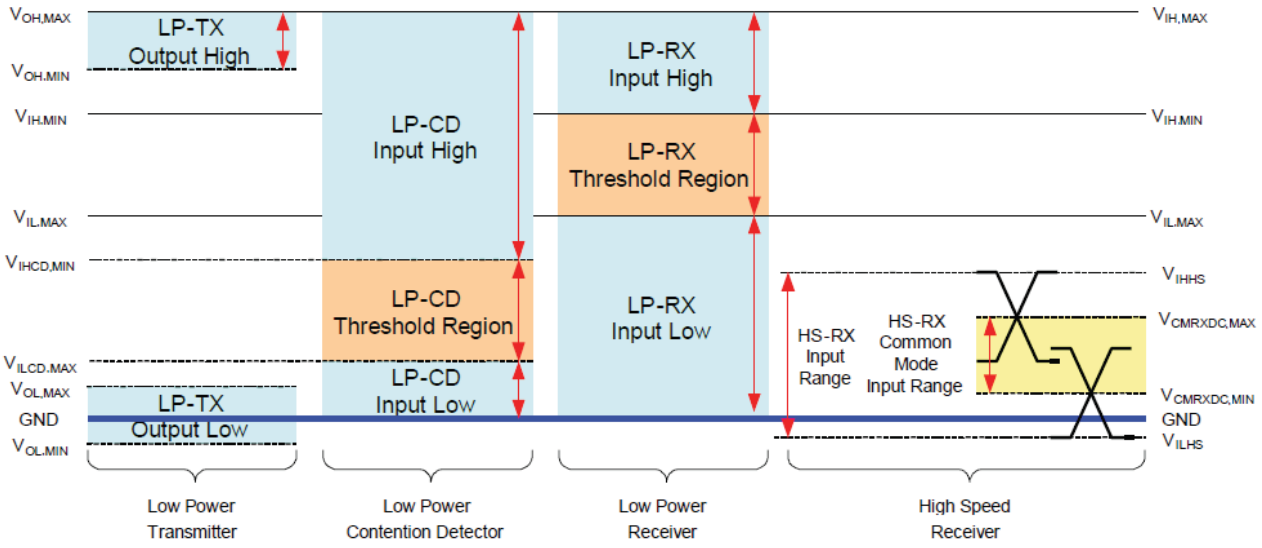


Note(2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note(3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note(4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 °C and I_L = 20 mA(Per EA) until the brightness becomes ≦ 50% of its original value.

4.4 MIPI DSI INPUT SIGNAL TIMING SPECIFICATIONS

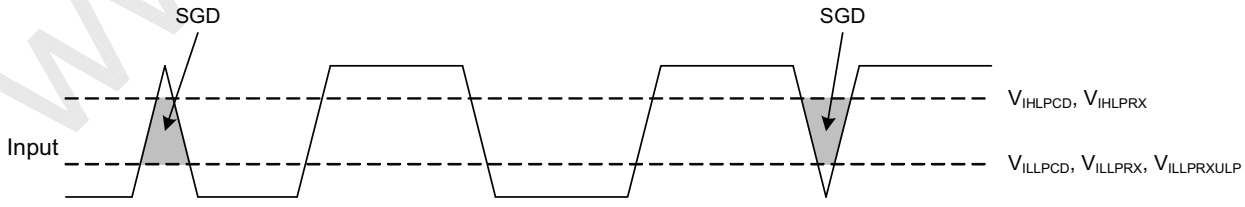


4.4.1 DC Electrical Characteristic

4.4.1.1 DC Characteristics for DSI LP Mode

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX (CLK, D0, D1)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX (CLK, D0, D1)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic low level output voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic high level input current	I_{IH}	LP-CD, LP-RX	-	-	10	μA
Logic low level input current	I_{IL}	LP-CD, LP-RX	-10	-	-	μA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	300	Vps

Note 1) VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V, Ta=-30 to 70 ºC (to +85 ºC no damage)
Note 2) DSI high speed is off.
Note 3) Peak interference amplitude max. 200mV and interference frequency min. 450MHz.

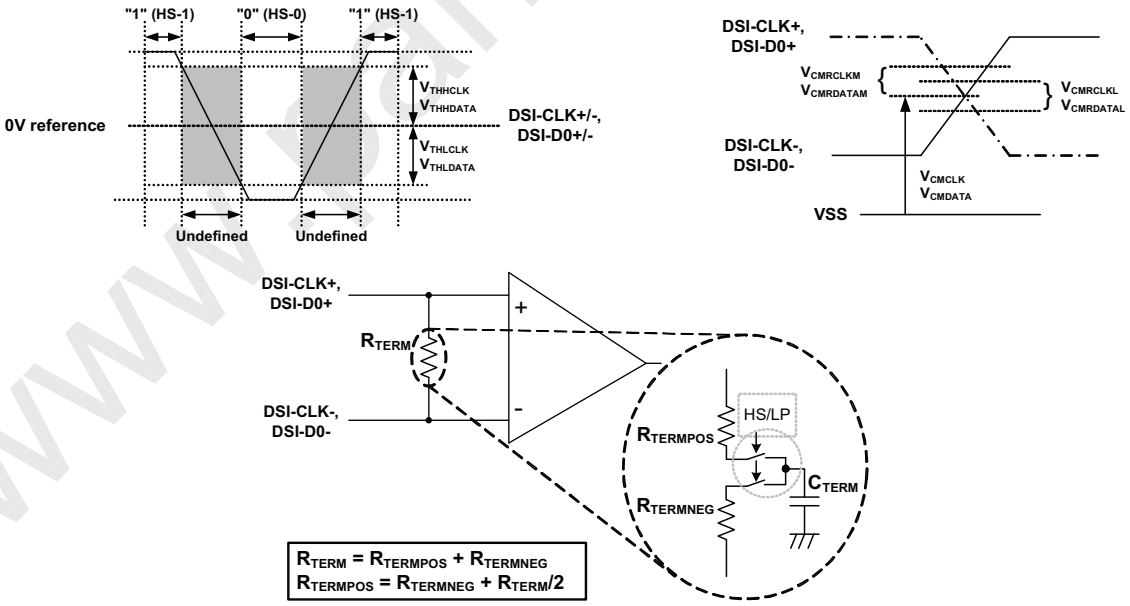


Spike/Glitch rejection-DSI

4.4.1.2 DC Characteristics for DSI HS Mode

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Input voltage common mode range	V_{CMCLK} V_{CMDATA}	DSI-CLK+/-, DSI-Dn+/- (Note2, 3)	70	-	330	mV
Input voltage common mode variation (≤ 450MHz)	$V_{CMRCLKL}$ $V_{CMRDATAL}$	DSI-CLK+/-, DSI-Dn+/- (Note 4)	-50	-	50	mV
Input voltage common mode variation (≥ 450MHz)	$V_{CMRCLKM}$ $V_{CMRDATAM}$	DSI-CLK+/-, DSI-Dn+/-	-	-	100	mV
Low-level differential input voltage threshold	V_{THLCLK} $V_{THLDATA}$	DSI-CLK+/-, DSI-Dn+/-	-70	-	-	mV
High-level differential input voltage threshold	V_{THHCLK} $V_{THHDATA}$	DSI-CLK+/-, DSI-Dn+/-	-	-	70	mV
Single-ended input low voltage	V_{ILHS}	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-40	-	-	mV
Single-ended input high voltage	V_{IHHS}	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	460	mV
Differential input termination resistor	R_{TERM}	DSI-CLK+/-, DSI-Dn+/-	80	100	125	Ω
Single-ended threshold voltage for termination enable	$V_{TERM-EN}$	DSI-CLK+/-, DSI-Dn+/-	-	-	450	mV
Termination capacitor	C_{TERM}	DSI-CLK+/-, DSI-Dn+/-	-	-	14	pF

Note 1) VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V, Ta=-30 to 70 ºC (to +85 ºC no damage).
Note 2) Includes 50mV (-50mV to 50mV) ground difference.
Note 3) Without $V_{CMRCLKM}$ / $V_{CMRDATAM}$.
Note 4) Without 50mV (-50mV to 50mV) ground difference.
Note 5) Dn=D0, D1, D2 and D3.



Differential voltage range, termination resistor and Common mode voltage

4.4.2 AC Electrical Characteristics

4.4.2.1 MIPI DSI Timing Characteristics

4.4.2.1.1 High Speed Mode

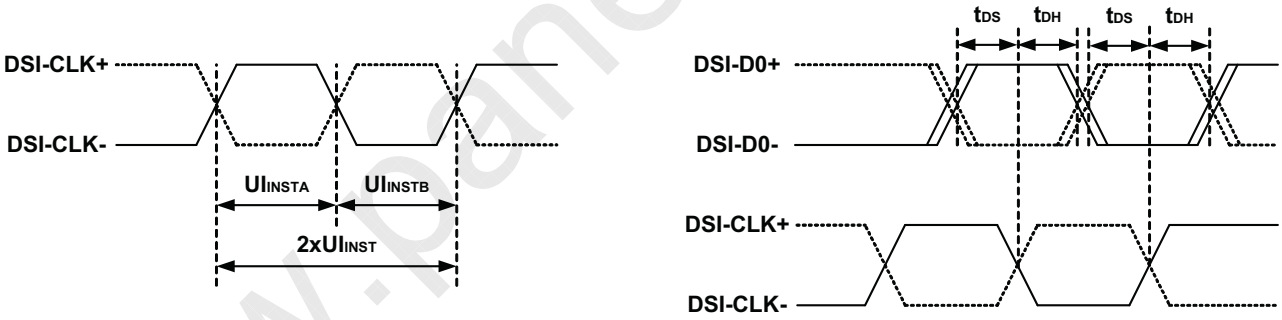
(*VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V* ,Ta = -30 to 70℃)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	4	-	8	ns	4 Lane (Note 2)
			3	-	8	ns	3 Lane (Note 2)
			2.352	-	8	ns	2 Lane (Note 3)
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs ($UI = UI_{INSTA} = UI_{INSTB}$)	2	-	4	ns	4 Lane (Note 2)
			1.5	-	4	ns	3 Lane (Note 2)
			1.176	-	4	ns	2 Lane (Note 3)
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15xUI	-	-	ps	
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15xUI	-	-	ps	
DSI-CLK+/-	t_{DRTCLK}	Differential rise time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	0.3xUI	ps	
DSI-CLK+/-	t_{DFTCLK}	Differential fall time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	0.3xUI	ps	

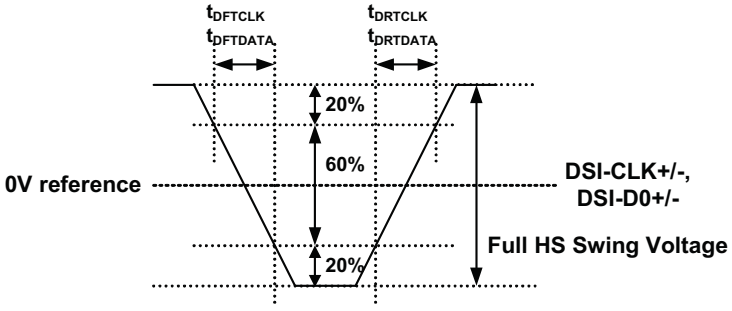
Note 1) Dn = D0, D1, D2 and D3.

Note 2) Maximum total bit rate is 2Gbps for 24-bit data format, 1.5Gbps for 18-bit data format and 1.33Gbps for 16-bit data format in 3 lanes or 4 lanes application which support to 800RGBx 1280 resolution.

Note 3) Maximum total bit rate is 1.7Gbps for 24-bit data format, 1.275Gbps for 18-bit data format and 1.13Gbps for 16-bit data format in 2 lanes application which support to 720RGBx1280 resolution.



DSI clock channel timing

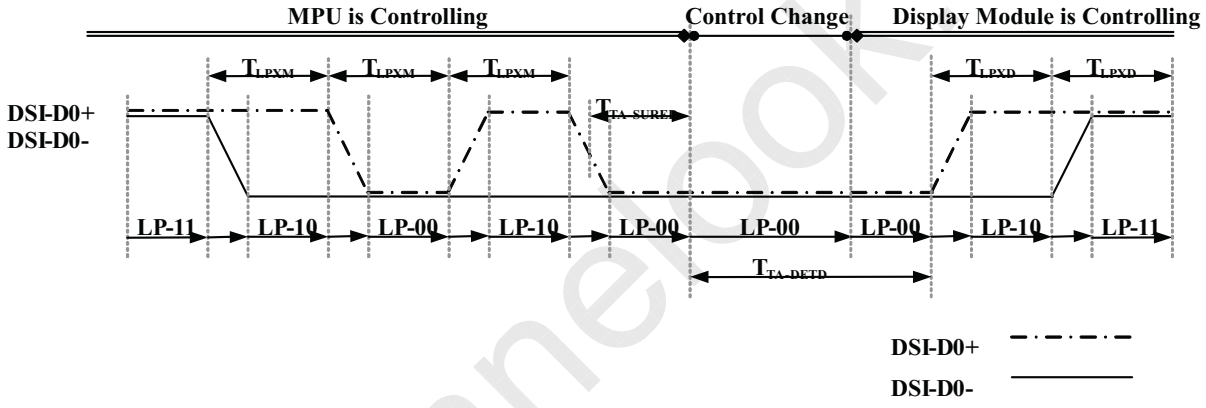


Rising and fall time on clock and data channel

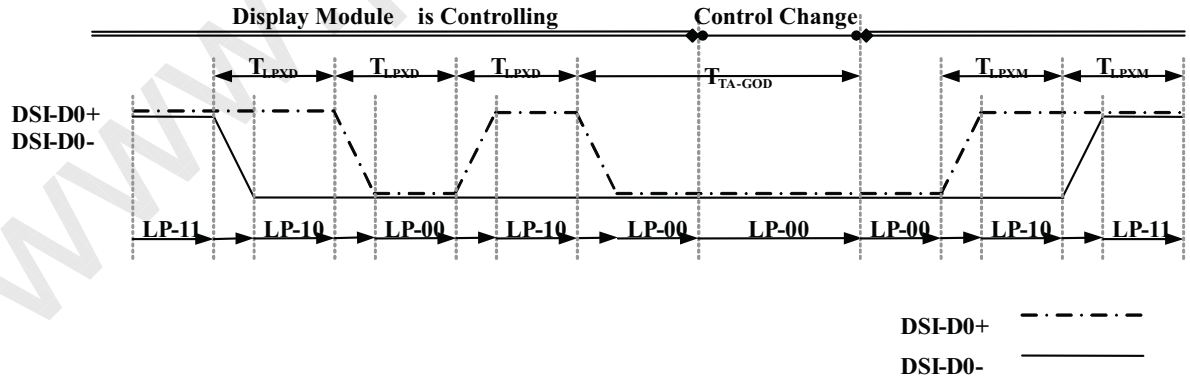
4.4.2.1.2 Low Power Mode

(*VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V*,Ta = -30 to 70℃)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module	50	-	75	ns	Input
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module → MPU	50	-	75	ns	Output
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T_{LPXD}	-	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by display module	$5xT_{LPXD}$	-	-	ns	Input
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	$4xT_{LPXD}$	-	-	ns	Output



Bus Turnaround (BAT) from MPU to display module Timing



Bus Turnaround (BAT) from display module to MPU Timing

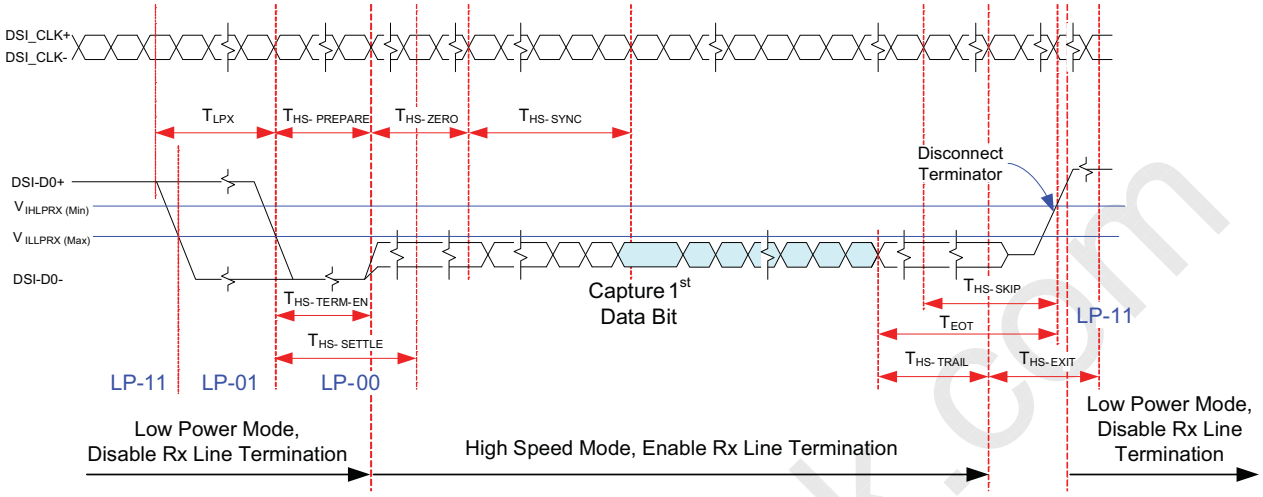
4.4.2.1.3 DSI Bursts

(*VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V*,Ta = -30 to 70℃)

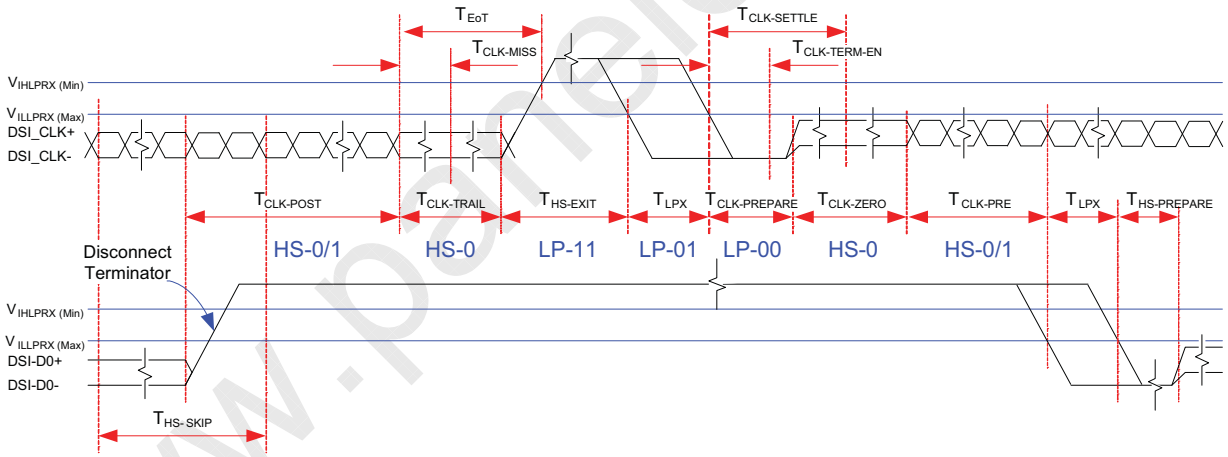
Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing							
DSI-Dn+/-	T_{LPX}	Length of any low power state period	50	-	-	ns	Input
DSI-Dn+/-	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40+4xUI	-	85+6xUI	ns	Input
DSI-Dn+/-	$T_{HS-TERM-EN}$	Time to enable data receiver line termination measured from when Dn crosses V_{ILMAX}	-	-	35+4xUI	ns	Input
High Speed Mode to Low Power Mode Timing							
DSI-Dn+/-	$T_{HS-SKIP}$	Time-out at display module to ignore transition period of EoT	40	-	55+4xUI	ns	Input
DSI-Dn+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-Dn+/-	$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4xUI	-	-	ns	Input
High Speed Mode to/from Low Power Mode Timing							
DSI-CLK+/-	$T_{CLK-POS}$	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+52xUI	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns	Input
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	-	95	ns	Input
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at clock lane display module to enable HS transmission	-	-	38	ns	Input
DSI-CLK+/-	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting clock	300	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8xUI	-	-	ns	Input

Note 1) Dn = D0, D1, D2 and D3.

Note 2) Two HS transmission can be sent with a break as short as $T_{HS-EXIT}$ from each other in continuous clock mode. In discontinuous mode, the break is longer which account $T_{CLK-POS}$, $T_{CLK-TRAIL}$ and $T_{HS-EXIT}$, before activity in clock and data lanes again.

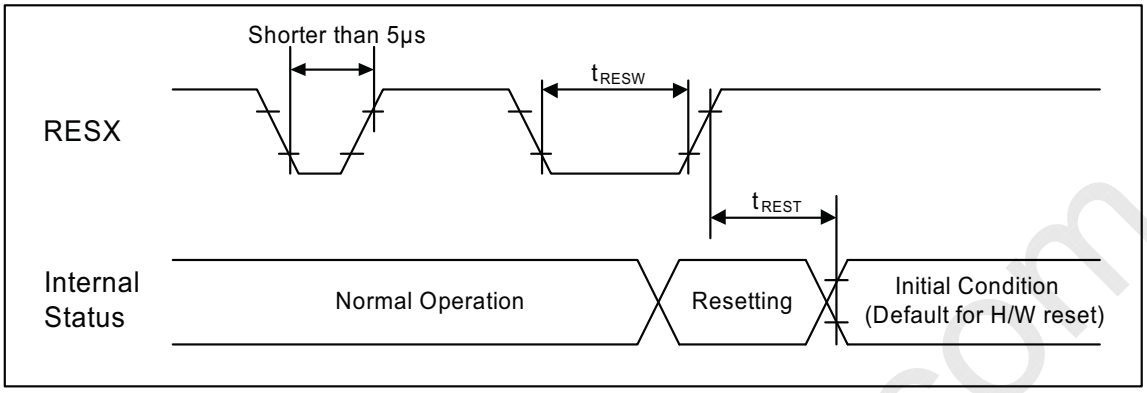


Data lanes-Low Power Mode to/from High Speed Mode Timing



Clock lanes- High Speed Mode to/from Low Power Mode Timing

4.4.2.2 Reset Input Timing



Reset input timing

(*VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V*,Ta = -30 to 70℃)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	tRESW	Reset "L" pulse width (Note 1)	10	-	-	µs	
	tREST	Reset complete time (Note 2)	-	-	5	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode and Note 5

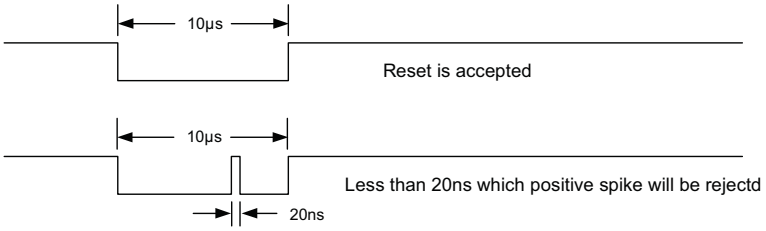
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	*Action*
Shorter than 5µs	*Reset Rejected*
Longer than 10µs	*Reset*
Between 5µs and 10µs	*Reset Start*

Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In–mode) and then return to Default condition for H/W reset.

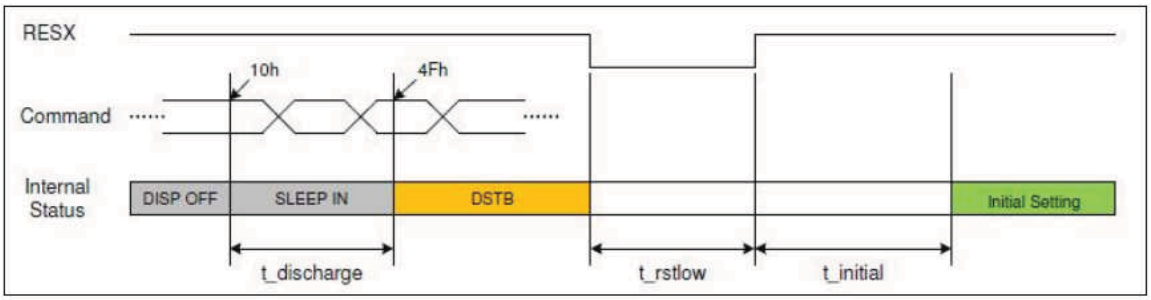
Note 3) During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

Note 4) Spike Rejection also applies during a valid reset pulse as shown below:



Note 5) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

4.4.2.3 Deep Standby Mode Timing



(*VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V*,Ta = -30 to 70℃)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	$t_{discharge}$	Sleep in into DSTB delay time	-	-	100	ms	
	t_{rstlow}	Reset low pulse	3	-	-	ms	
	$t_{initial}$	Reset high to initial setting delay time	-	-	120	ms	

Note 1) t_discharge suggested delay time over 100ms.

Note 2) t_initial suggested delay time over 120ms.

4.5 MIPI interface (Mobile Industry Processing Interface)

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.
DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode.

Note: The product only supports Video Mode operation.
Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

4.5.1 MIPI Lane Configuration

	MCU (Master) Display Module (Slave)
Clock Lane+/-	Unidirectional Lane ■ Clock Only ■ Escape Mode(ULPS Only)
Data Lane0+/-	Bi-directional Lane ■ Forward High-Speed ■ Bi-directional Escape Mode ■ Bi-directional LPDT
Data Lane1+/-	Unidirectional ■ Forward High speed
Data Lane2+/-	Unidirectional ■ Forward High speed
Data Lane3+/-	Unidirectional ■ Forward High speed

The connection between host device and display module is as reference.

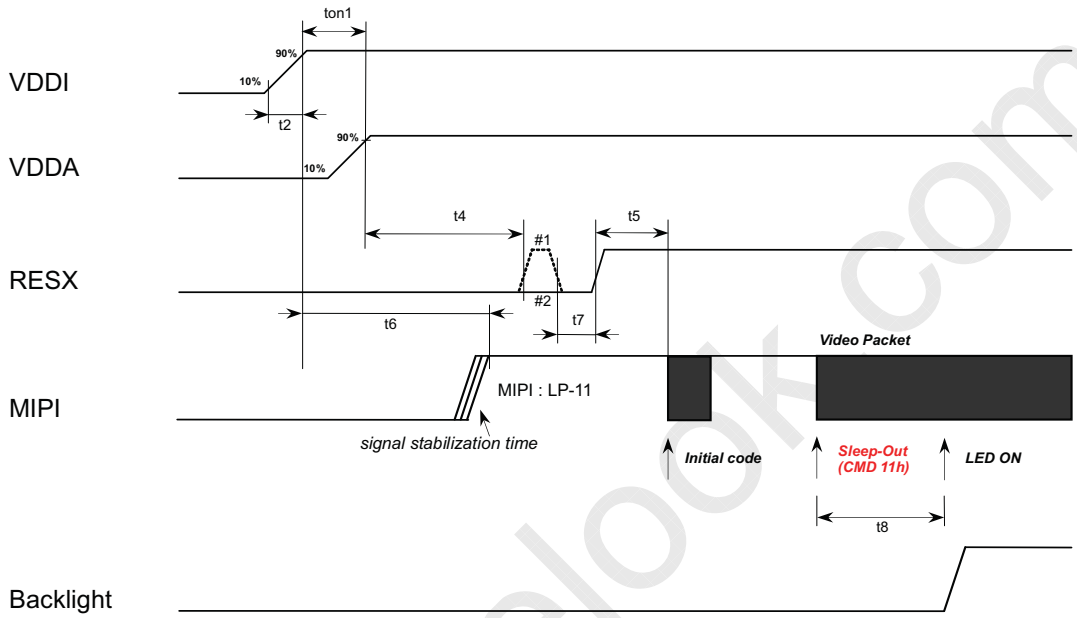
Note: Usually, we suggest host can use non-continuous clock mode & non-burst mode with sync events to transmit the video stream to enhance ESD ability.

4.6 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram.

a. Power on:

VDDI=1.7~1.9V, VCI(VDDA)=3.0 to 3.6V



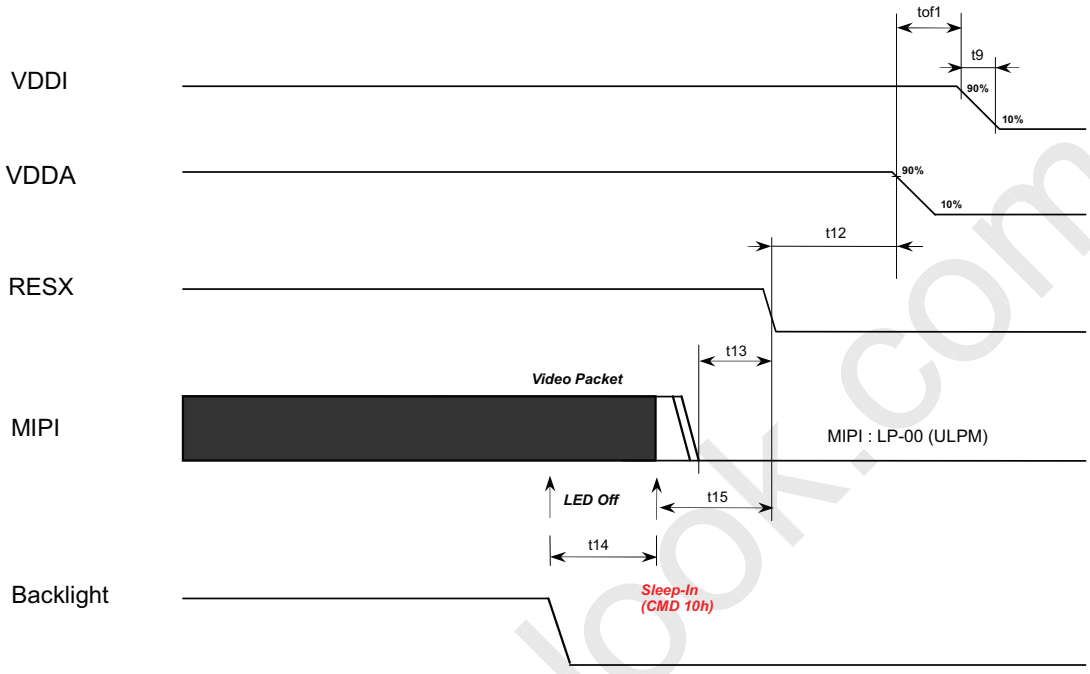
Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Note 2: Reset signal H to L to H (#1) is better than only L to H (#2).

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
ton1	0	-	-	ms	
t2	-	No limit	-	µs	
t4	40	-	-	ms	
t5	20	-	-	ms	
t6	0	-	t4	ms	
t7	10	-	-	µs	
t8	8	-	-	VS	Keep data more than 8 frames (VS)

b. Power off:

VDDI=1.7~1.9V, VCI(VDDA)=3.0 to 3.6V



Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
t9	150	-	-	μs	
tof1	0	-	-	ms	
t12	0	-	-	ms	
t13	0	-	-	ms	
t14	0	-	-	ms	
t15	100	-	-	ms	

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

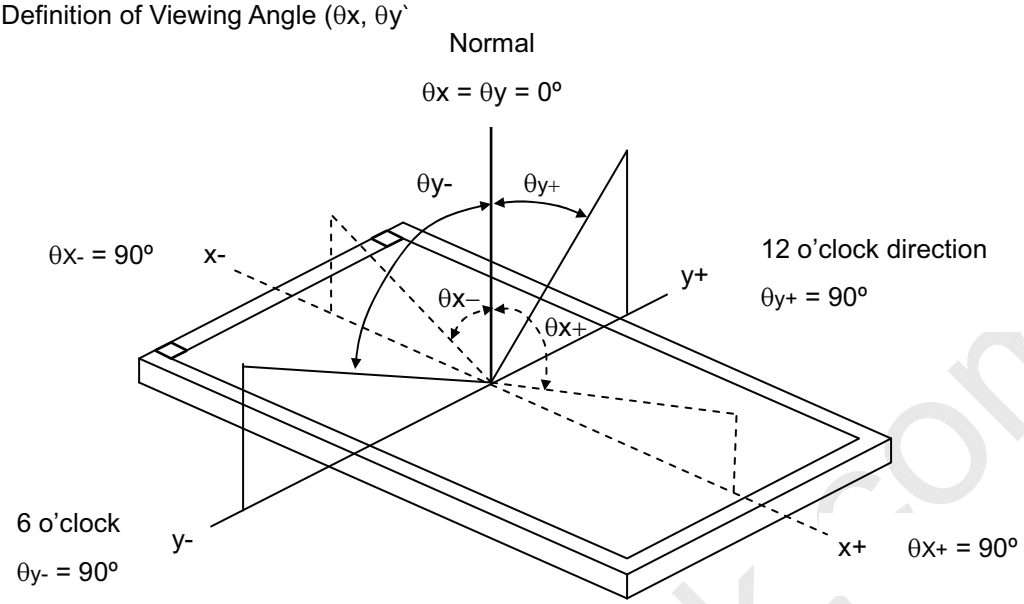
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VDDI	1.8	V
	VCI	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I_L	20	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	600	800	-	-	(2), (5) ,(7)
Response Time		T_R+T_F		-	25	30	ms	(3) ,(7)
CP Luminance of White		L_{CP}		300	350	-	Cd/m^2	(4), (6) ,(7)
Color Coordinate	White	Wx		Typ – 0.03	0.313	Typ + 0.03	-	(4), (6) ,(7)
		Wy			0.329			
	R	Rx			0.618			
		Ry			0.340			
	G	Gx			0.344			
		Gy			0.600			
	B	Bx			0.160			
		By			0.074			
NTSC		%		55	60			(2). (5).(7)
White Variation		5 point	θ_x=0°, θ_Y =0°	80			%	(5). (6) .(7)
		13 point		67				
Flicker		dB				-30		(8)
Crosstalk		%				2		(9)
Gamma			θ_x=0°, θ_Y =0°	2.0	2.2	2.4		
Viewing Angle	Horizontal	θx- + θx+	CR>10	170	178	-	Deg.	(1),(5) ,(7)
	Vertical	θy- + θy+		170	178	-		

Note(1) Definition of Viewing Angle (θx, θy`



Note(2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255 / L0

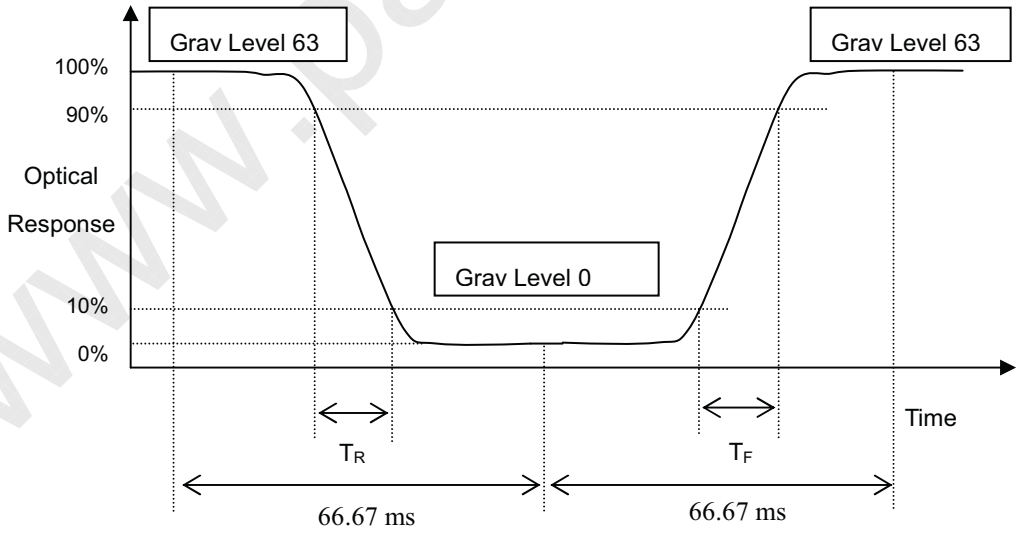
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note(3) Definition of Response Time (T_R, T_F):



Note(4) Definition of Center Point Luminance of White (L_{CP}):

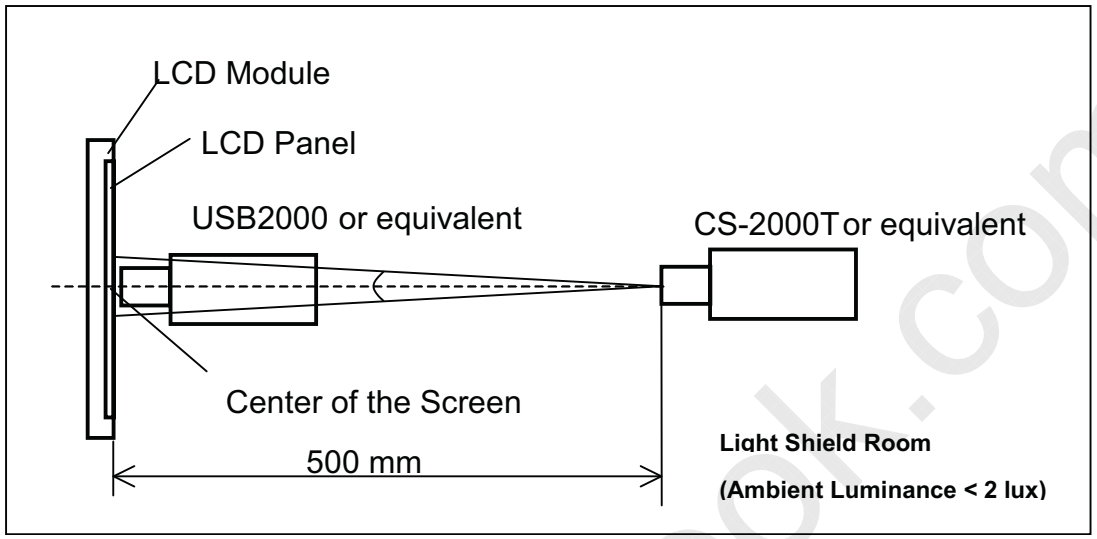
Measure the luminance of gray level 63 at center point

L_{CP} = L(5)

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note(5) Measurement Setup:

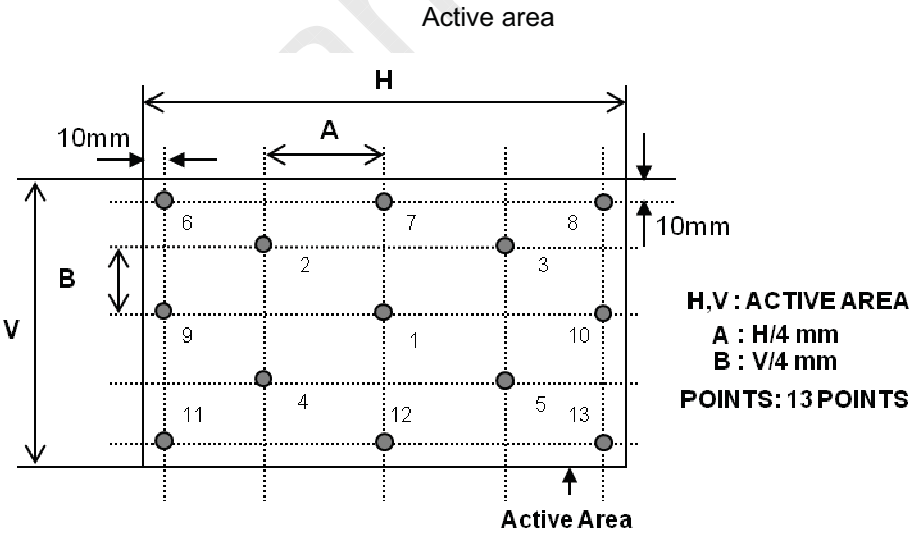
The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note(6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 13 points

δW_{9p} = {Minimum [L (1) ~ L (13)] / Maximum [L (1) ~ L (13)]}*100%



Note(7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

Note(8) Flicker

No visual flicker will be allowed. The flicker level should be measured on GS127, The output signal is measured by Minolta CA210 immediately while Vcom is optimized. The flicker is essentially a ratio of the Amplitude in the frequency spectrum at 30 Hz (A30) and 0 Hz (A0), i.e.,

$$F = 20 \text{ Log } (A30 / A0).$$

Note(9) Crosstalk

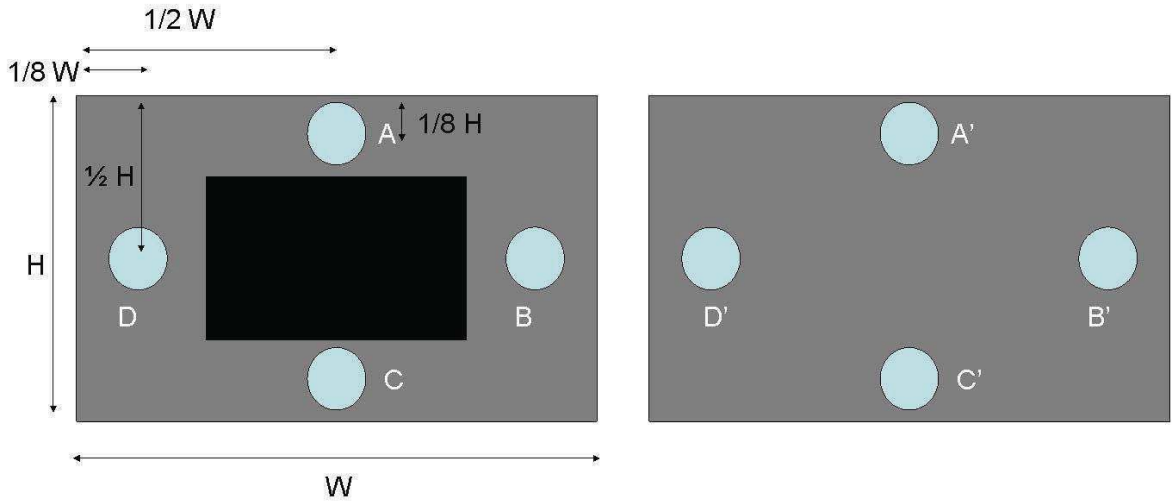
No visual cross-talk will be allowed. Two luminance values are measured at the same position (i.e. A and A'). The cross-talk, is defined as,

$$C(A, B, C, D) = | (L(A', B', C', D') - L(A, B, C, D))/L(A, B, C, D) | \cdot 100\%,$$

Where, L(A, B, C, D) = Luminance in Position A, B, C, D

L(A', B', C', D') = Luminance in Position A', B', C', D'

Crosstalk=max (C(A), C(B), C(C), C(D))



Background : GS 127

Center Pattern: GS 0, 50%(W) x 50%(H).

6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	70℃, 240 hours	(1) (2)
Low Temperature Storage Test	-20℃, 240 hours	
Thermal Shock Storage Test	-20℃, 0.5hour←→70℃, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	60℃, 240 hours	
Low Temperature Operation Test	-10℃, 240 hours	
High Temperature & High Humidity Operation Test	60℃, RH 90%, 240hours	
ESD Test (Operation)	Condition 1 : Contact Discharge, ±8KV Condition 2 : Air Discharge, ±12KV	(1)
Shock (Non-Operating)	220G, 2ms, half sine wave,1 time for each direction of ±X,±Y,±Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

Note(1) Criteria : Normal display image with no obvious non-uniformity and no line defect.
(should be checked with 8% ND filter and within 45° viewing angle from vertical)

Note(2) Evaluation should be tested after storage at room temperature for more than two hour

Note(3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

7. PACKING

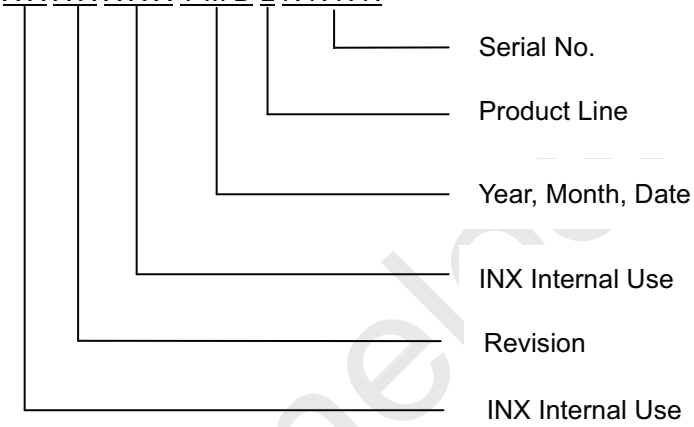
7.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

(a) Model Name: N080ICE – GB1

(b) Revision: Rev. XX, for example: C1, C2 …etc.

(c) Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

(a) Manufactured Date: Year: 0~9, for 2010~2019

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

7.2 CARTON

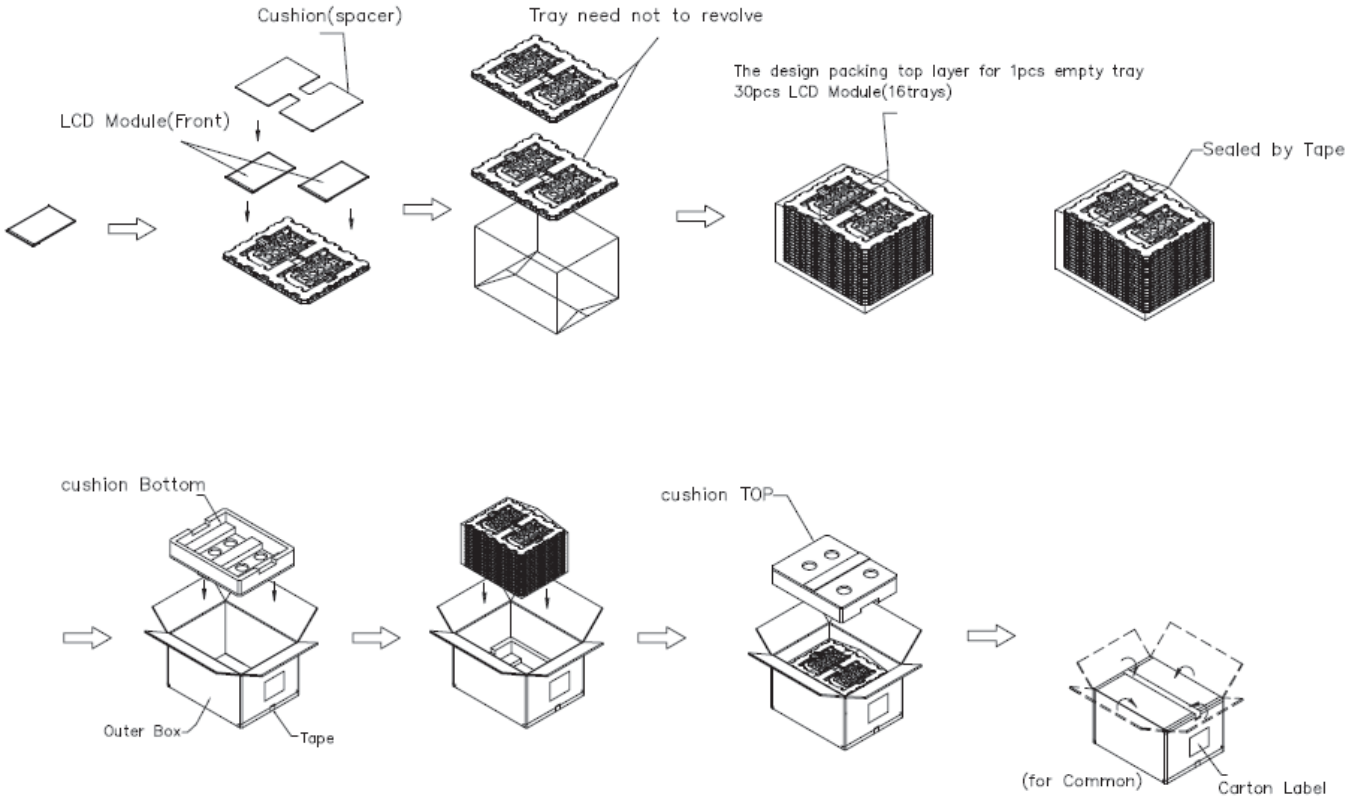


Figure. 7-1 Packing method

7.3 PALLET

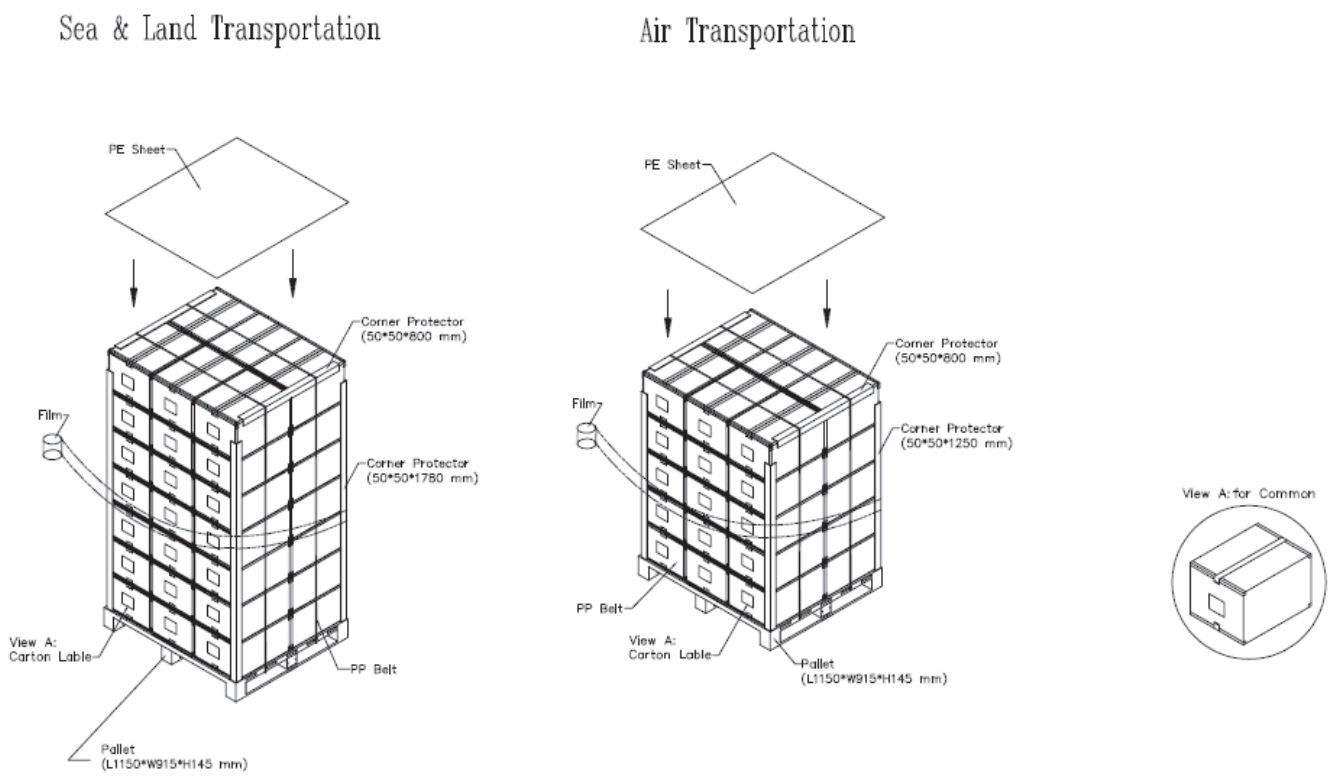


Figure. 7-2 Packing method

7.4 Un-Packing

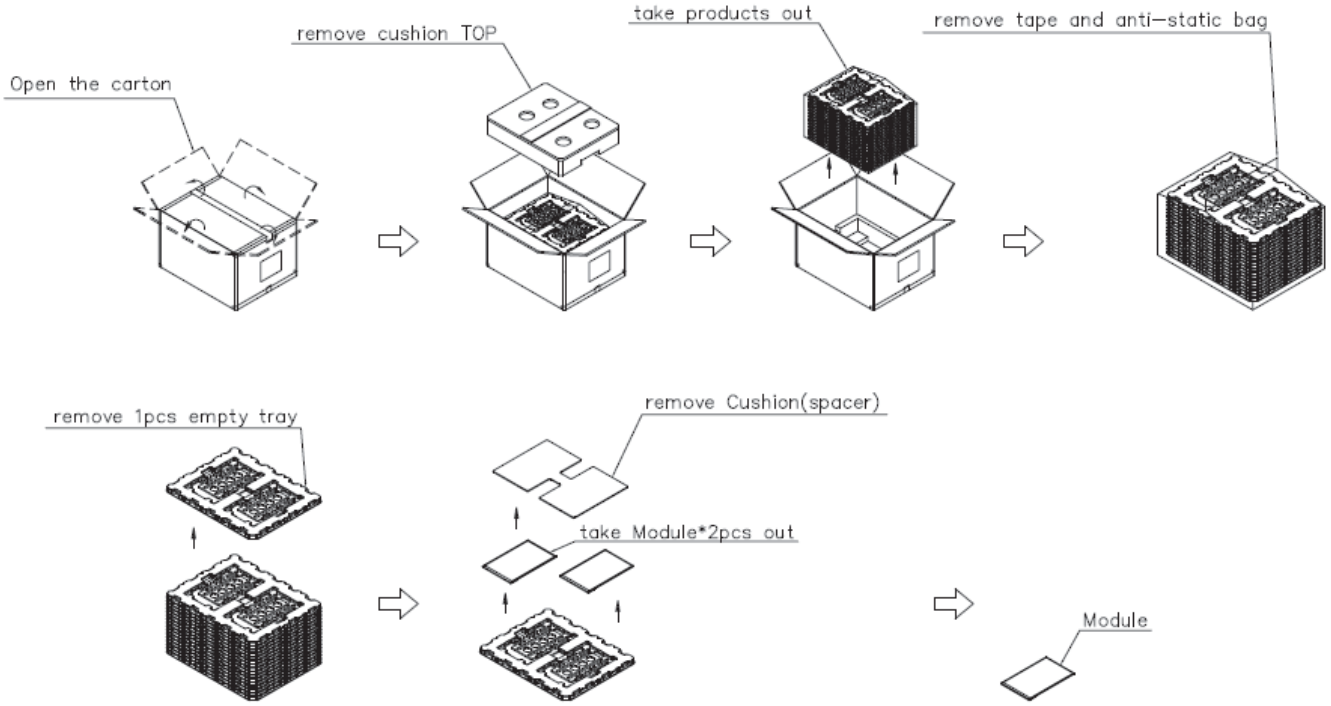
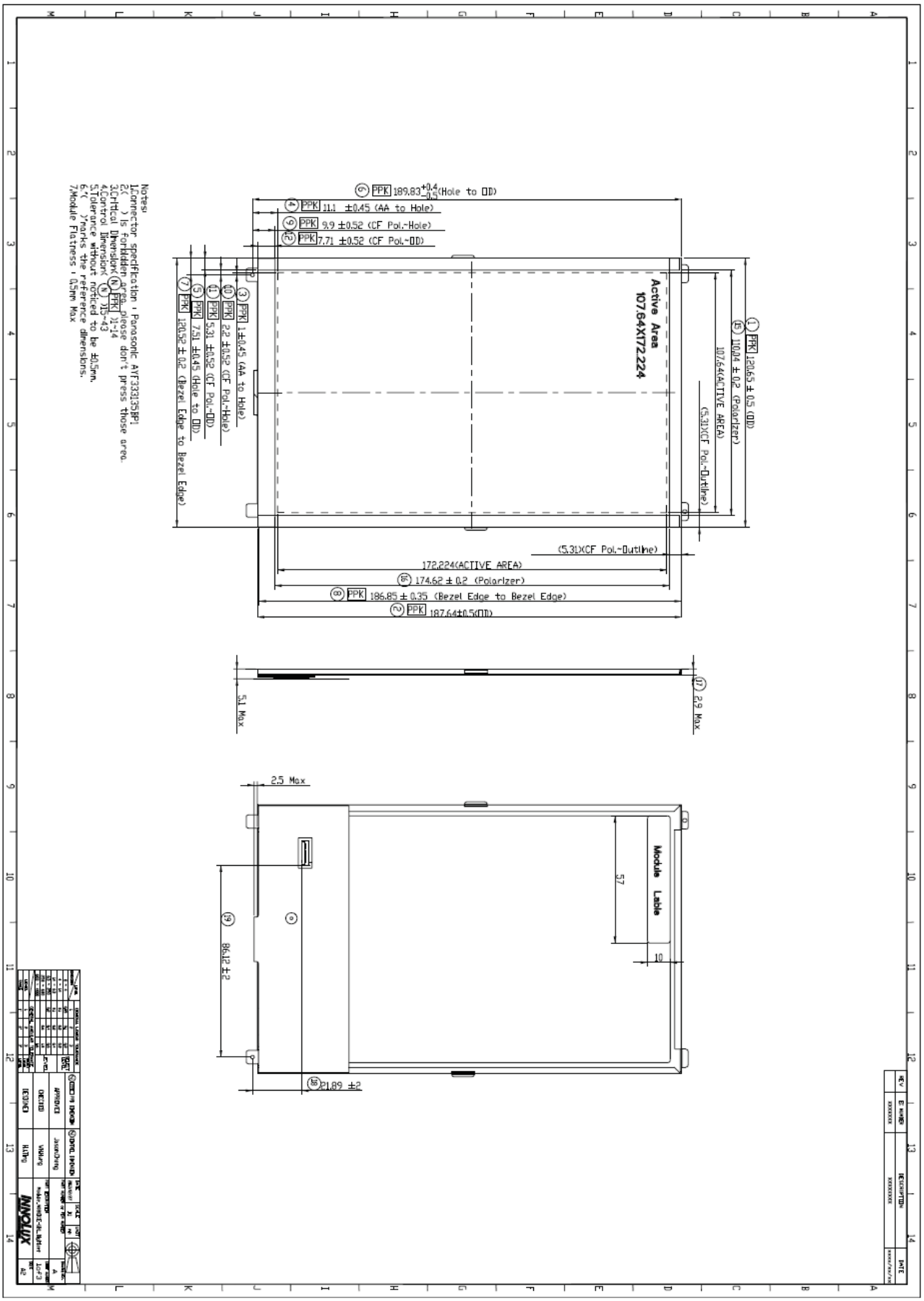
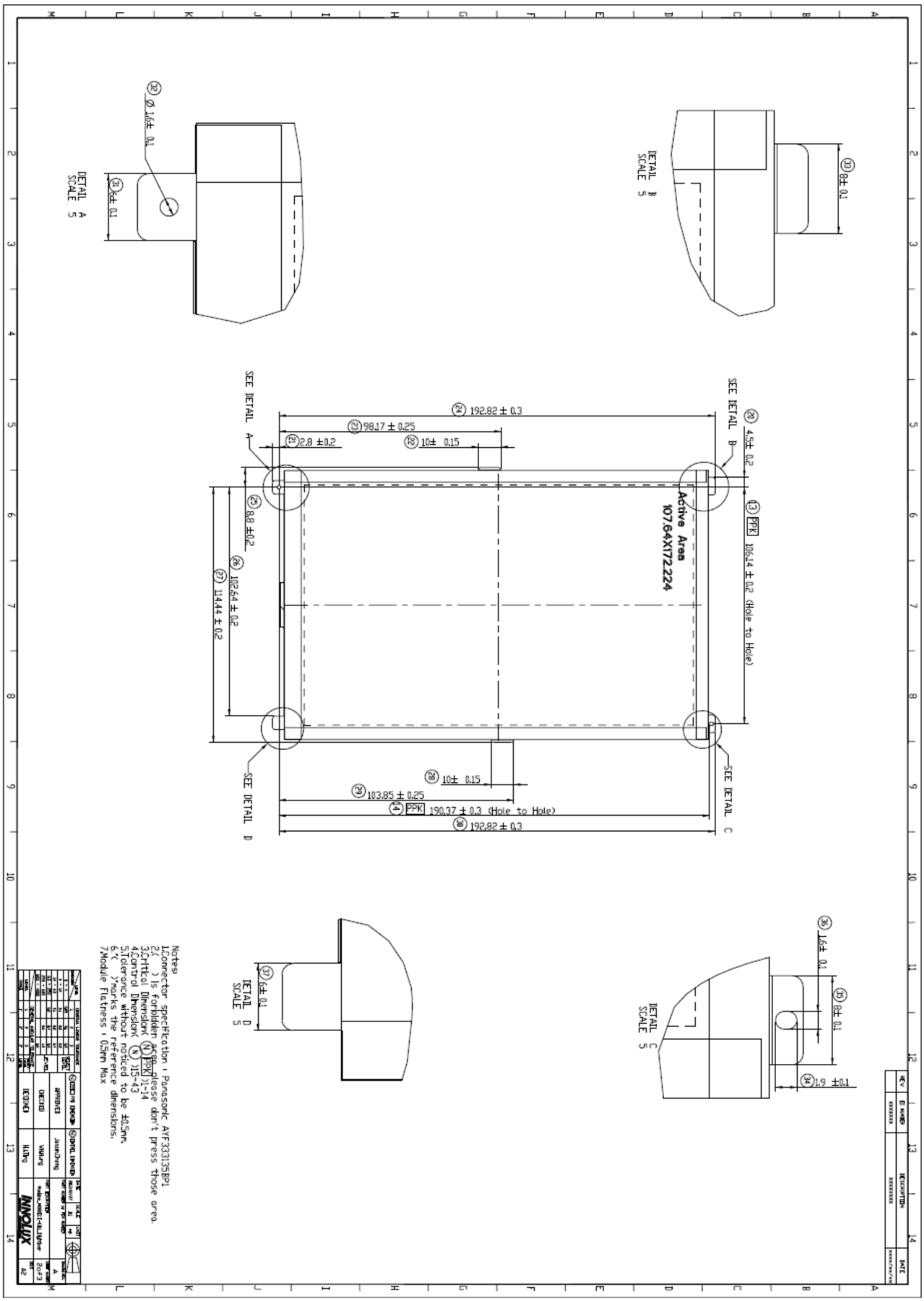
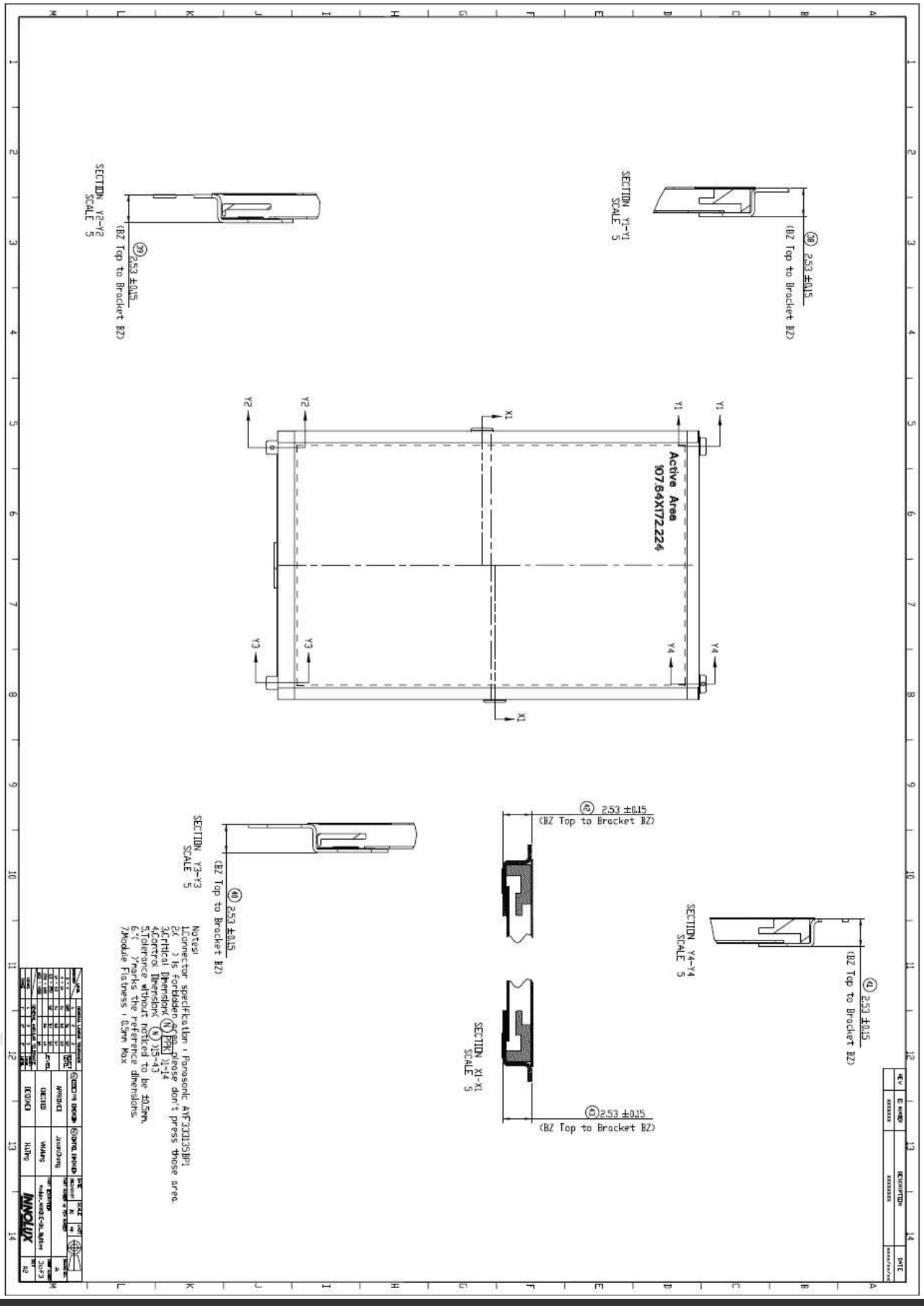


Figure. 7-3 Un-Packing method

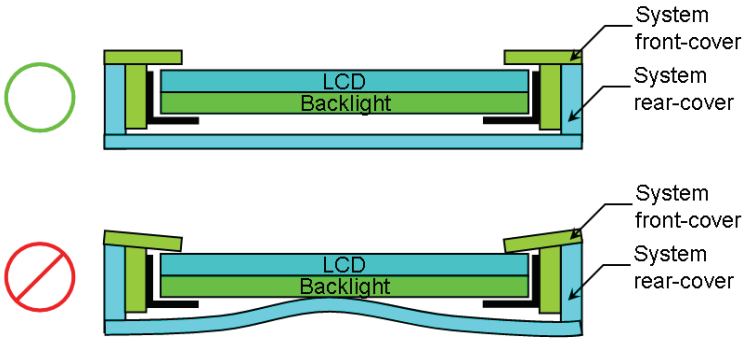
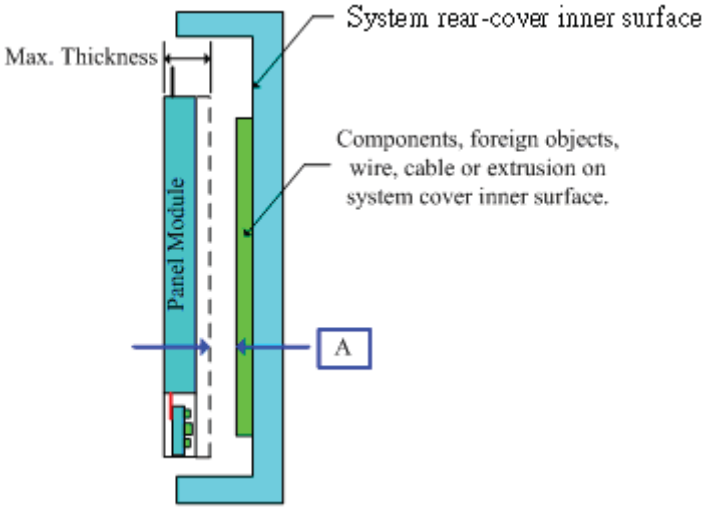
Appendix I. OUTLINE DRAWING (Label position will be updated as requirement)

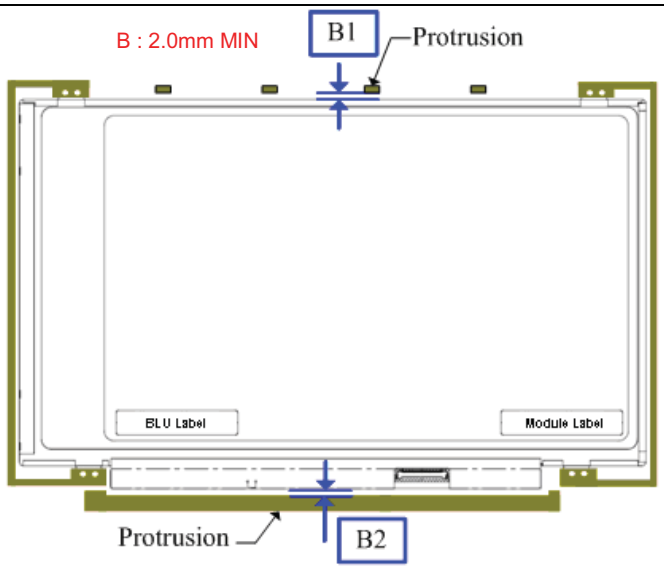




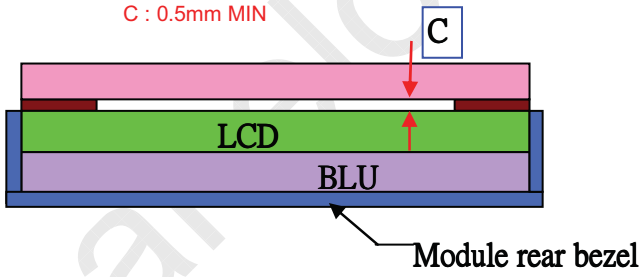


Appendix II. SYSTEM COVER DESIGN GUIDANCE

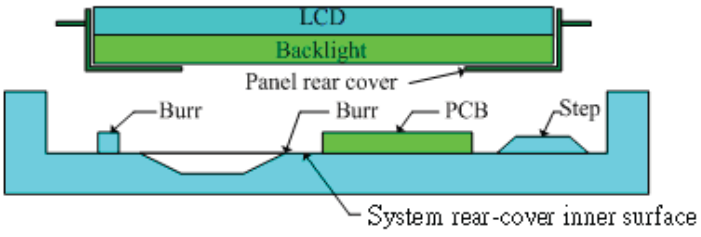
1.	**Permanent deformation of system cover after reliability test**
	
Definition	System cover including front and rear cover may deform during reliability test. Permanent deformation of system front and rear cover after reliability test should not interfere with panel. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack.
2.	**Design gap A between panel & any components on system rear-cover**
	
Definition	Gap between panel's maximum thickness boundary & system's inner surface components such as wire, cable, extrusion is needed for preventing from backpack or pogo test fail. Because zero gap or interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, and cell crack may occur. Flatness of panel and system rear-cover should be taken into account for gap design.
3	**Design gap B1 & B2 between panel & protrusions**



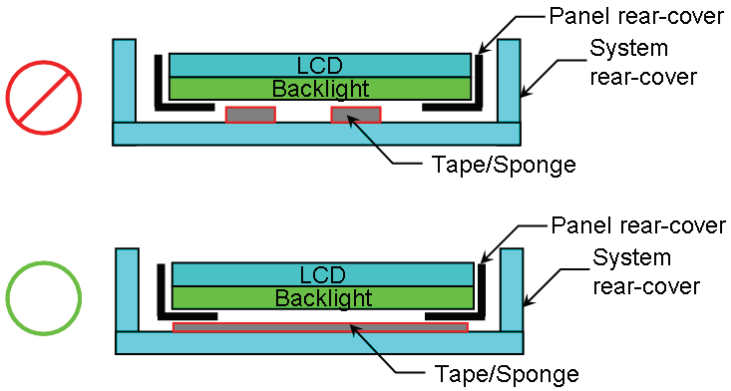
Definition	Gap between panel & protrusions is needed to prevent shock test failure. Because protrusions with small gap may hit panel during the test. Issue such as cell crack, abnormal display may occur.
4	**Design gap C between touch panel & panel surface.**



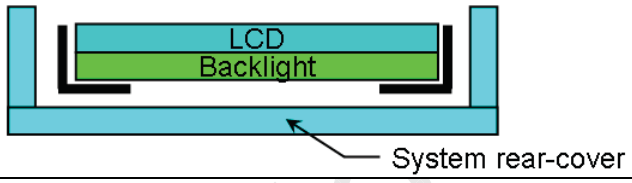
Definition	Air gap design between touch panel & panel surface is needed to prevent pooling, newton ring or glass broken. Compression ration of double side tape may cause pooling issue or newton ring. This phenomenon is obvious during pooling inspection procedure. To remain sufficient gap between touch panel and panel surface is recommended.
5	**System rear-cover inner surface examination**



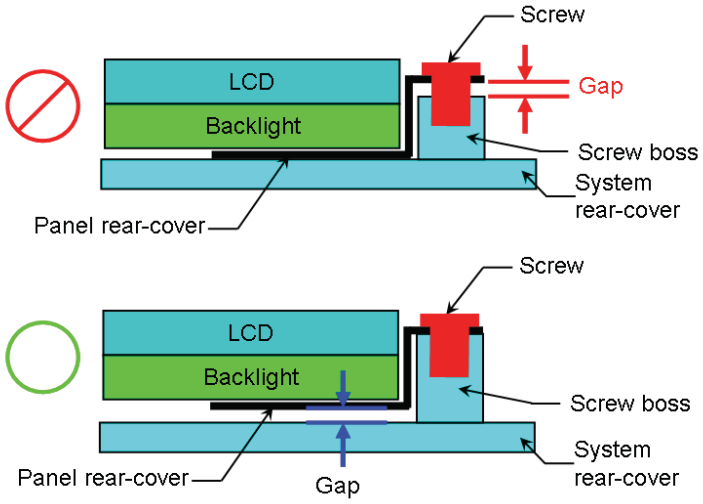
Definition	Burr at logo edge, steps, protrusions or PCB board may cause stress concentration. White spot or glass broken issue may occur during reliability test.
6	**Tape/sponge design on system inner surface**



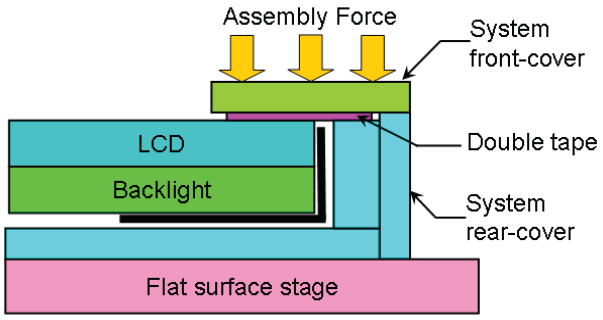
Definition	To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, tape/sponge should be well covered under panel rear-cover. Because tape/sponge in separate location may act as pressure concentration location.
7	**Material used for system rear-cover**



Definition	System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test, or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Pooling issue may occur because screw's boss positioning for module's bracket are deformed during open-close test. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.
8	**Screw boss height design**



Definition	Screw boss height should be designed with respect to the height of bracket bottom surface to panel bottom surface + flatness change of panel itself. Because gap will exist between screw boss and bracket, if the screw boss height is smaller. As result while fastening screw, bracket will deformed and pooling issue may occur.
9	**Assembly SOP examination for touch panel with double side tape design**

	
Definition	To prevent panel crack during touch panel assembly process with double tape design, it is only allowed to give slight pressure with large contact area. This can help to distribute the stress and prevent stress concentration. We also suggest putting the system on a flat surface stage to prevent unequal stress distribution during the assembly.

Appendix III. NT35521 REGISTER SETTING

```
REGW 0xFF,0xAA,0x55,0xA5,0x80
//========== Internal setting ==========
REGW 0x6F,0x11,0x00
REGW 0xF7,0x20,0x00
REGW 0x6F,0x06
REGW 0xF7,0xA0
REGW 0x6F,0x19
REGW 0xF7,0x12

REGW 0x6F,0x08
REGW 0xFA,0x40
REGW 0x6F,0x11
REGW 0xF3,0x01

//========== page0 relative ==========
REGW 0xF0,0x55,0xAA,0x52,0x08,0x00
REGW   0xC8, 0x80

REGW 0xB1,0x6C,0x01

REGW 0xB6,0x08

REGW 0x6F,0x02
REGW 0xB8,0x08

REGW 0xBB,0x74,0x44

REGW 0xBC,0x00,0x00

REGW   0xBD, 0x02,0xB0,0x0C,0x0A,0x00

//========== page1 relative ==========
REGW 0xF0,0x55,0xAA,0x52,0x08,0x01

REGW 0xB0,0x05,0x05
```

REGW 0xB1,0x05,0x05

REGW 0xBC,0x90,0x01
REGW 0xBD,0x90,0x01

REGW 0xCA,0x00

REGW 0xC0,0x04

REGW 0xBE,0x29

REGW 0xB3,0x37,0x37
REGW 0xB4,0x19,0x19

REGW 0xB9,0x44,0x44
REGW 0xBA,0x24,0x24

//========== page2 relative ==========
REGW 0xF0,0x55,0xAA,0x52,0x08,0x02

REGW 0xEE,0x01
REGW 0xEF,0x09,0x06,0x15,0x18

regw 0xB0,0x00,0x00,0x00,0x25,0x00,0x43
regw 0x6F,0x06
regw 0xB0,0x00,0x54,0x00,0x68,0x00,0xA0
regw 0x6F,0x0C
regw 0xB0,0x00,0xC0,0x01,0x00
regw 0xB1,0x01,0x30,0x01,0x78,0x01,0xAE
regw 0x6F,0x06
regw 0xB1,0x02,0x08,0x02,0x50,0x02,0x52
regw 0x6F,0x0C
regw 0xB1,0x02,0x96,0x02,0xDC
regw 0xB2,0x03,0x08,0x03,0x49,0x03,0x77
regw 0x6F,0x06
regw 0xB2,0x03,0xA3,0x03,0xAC,0x03,0xC2
regw 0x6F,0x0C

regw 0xB2,0x03,0xC9,0x03,0xE3
regw 0xB3,0x03,0xFC,0x03,0xFF

// PAGE6 : GOUT Mapping, VGLO select
regw 0xF0, 0x55,0xAA,0x52,0x08,0x06
regw 0xB0, 0x00,0x10
regw 0xB1, 0x12,0x14
regw 0xB2, 0x16,0x18
regw 0xB3, 0x1A,0x29
regw 0xB4, 0x2A,0x08
regw 0xB5, 0x31,0x31
regw 0xB6, 0x31,0x31
regw 0xB7, 0x31,0x31
regw 0xB8, 0x31,0x0A
regw 0xB9, 0x31,0x31
regw 0xBA, 0x31,0x31
regw 0xBB, 0x0B,0x31
regw 0xBC, 0x31,0x31
regw 0xBD, 0x31,0x31
regw 0xBE, 0x31,0x31
regw 0xBF, 0x09,0x2A
regw 0xC0, 0x29,0x1B
regw 0xC1, 0x19,0x17
regw 0xC2, 0x15,0x13
regw 0xC3, 0x11,0x01
regw 0xE5, 0x31,0x31
regw 0xC4, 0x09,0x1B
regw 0xC5, 0x19,0x17
regw 0xC6, 0x15,0x13
regw 0xC7, 0x11,0x29
regw 0xC8, 0x2A,0x01
regw 0xC9, 0x31,0x31
regw 0xCA, 0x31,0x31
regw 0xCB, 0x31,0x31
regw 0xCC, 0x31,0x0B
regw 0xCD, 0x31,0x31
regw 0xCE, 0x31,0x31

```
regw   0xCF, 0x0A,0x31
regw   0xD0, 0x31,0x31
regw   0xD1, 0x31,0x31
regw   0xD2, 0x31,0x31
regw   0xD3, 0x00,0x2A
regw   0xD4, 0x29,0x10
regw   0xD5, 0x12,0x14
regw   0xD6, 0x16,0x18
regw   0xD7, 0x1A,0x08
regw   0xE6, 0x31,0x31
regw   0xD8, 0x00,0x00,0x00,0x54,0x00
regw   0xD9, 0x00,0x15,0x00,0x00,0x00
regw   0xE7, 0x00

// PAGE3 :
regw   0xF0, 0x55,0xAA,0x52,0x08,0x03
regw   0xB0, 0x20,0x00
regw   0xB1, 0x20,0x00
regw   0xB2, 0x05,0x00,0x00,0x00,0x00

regw   0xB6, 0x05,0x00,0x00,0x00,0x00
regw   0xB7, 0x05,0x00,0x00,0x00,0x00

regw   0xBA, 0x57,0x00,0x00,0x00,0x00
regw   0xBB, 0x57,0x00,0x00,0x00,0x00

regw   0xC0, 0x00,0x00,0x00,0x00
regw   0xC1, 0x00,0x00,0x00,0x00

regw   0xC4, 0x60
regw   0xC5, 0x40

// PAGE5 :
regw   0xF0, 0x55,0xAA,0x52,0x08,0x05
regw   0xBD, 0x03,0x01,0x03,0x03,0x03
regw   0xB0, 0x17,0x06
regw   0xB1, 0x17,0x06
```

```
regw   0xB2, 0x17,0x06
regw   0xB3, 0x17,0x06
regw   0xB4, 0x17,0x06
regw   0xB5, 0x17,0x06

regw   0xB8, 0x00
regw   0xB9, 0x00
regw   0xBA, 0x00
regw   0xBB, 0x02
regw   0xBC, 0x00

regw   0xC0, 0x07

regw   0xC4, 0x80
regw   0xC5, 0xA4

regw   0xC8, 0x05,0x30
regw   0xC9, 0x01,0x31

regw   0xCC, 0x00,0x00,0x3C
regw   0xCD, 0x00,0x00,0x3C

regw   0xD1, 0x00,0x04,0xFD,0x07,0x10
regw   0xD2, 0x00,0x05,0x02,0x07,0x10

regw   0xE5, 0x06
regw   0xE6, 0x06
regw   0xE7, 0x06
regw   0xE8, 0x06
regw   0xE9, 0x06
regw   0xEA, 0x06

regw   0xED, 0x30

REGW 0x6F,0x11
REGW 0xF3,0x01
```

regw 0x35

regw 0x11

regw 0x29