INNOLUX 群創光電

# PRODUCT SPECIFICATION

**Doc. Number:**

☐ Tentative Specification

■ Preliminary Specification

☐ Approval Specification

# MODEL NO: JJ070IA-18L
# SUFFIX:

**Customer:**

**APPROVED BY**

**Name / Title**

**Note :**

**Please return 1 copy for your confirmation with your signature and comments.**

| Approved By | Checked By | Prepared By |
|---|---|---|
| HENRY.CHIEN<br>HUAI.CHANG | KAY.LIU<br>MEG.CHU | EDDY.CHANG |

# REVISION HISTORY

| Version | Date | Page | Description |
|---|---|---|---|
| 0.1 | Jan,14,2019 | All | Spec Ver0.1 was first issued |

# Contents

# 1. General Specifications

| No. | Item | Specification | Remark |
|---|---|---|---|
| 1 | LCD Size | 7 inch (Diagonal) | |
| 2 | Driver Element | a-Si TFT Active Matrix | |
| 3 | Resolution | 800 X 3(RGB) X 480 | |
| 4 | Display Mode | Normally Black, Transmissive | |
| 5 | Dot Pitch | 0.1905(W) x 0.1905(L) mm | |
| 6 | Active Area | 152.4 mm(H) x 91.44 mm(V) | |
| 7 | Module Size | 162.8(W) X 104.84(H) X 5.5(D) mm | Note 1-1 |
| 8 | Bezel Opening Size | 155.4(W) X 94.44(H) mm | |
| 9 | Surface Treatment | Anti-Glare | |
| 10 | Color Arrangement | RGB-Stripe | |
| 11 | Interface | LVDS (DE only) | Note 1-2 |
| 12 | Backlight Power Consumption | 3.224 W (Typ.) | |
| 13 | Panel Power Consumption | 450 mW (Typ, @ White Pattern) | |
| 14 | Weight | 195g ;+/- 5% (Max.) | |

**Note 1-1: Refer to Mechanical Drawing.**

**Note 1-2: LVDS, 8-bit, JEIDA format**

# 2. Pin Assignment

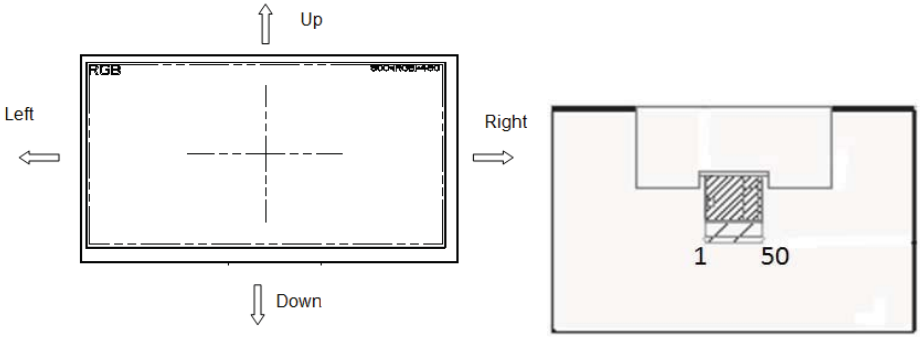
**Connector on PCB is used for the module electronics interface. The recommended model is IMSA-12003S-50A-GFN4 manufactured by IRISO.**

| JJ070IA-18E main FPCa golden finger pin define | | | |
|---|---|---|---|
| **PIN NO.** | **Symbol** | **I/O/P** | **Function** |
| **1** | NTC_GND | P | LED Driver for NTC Function, If not use please keep floating or connect to ground. |
| **2** | LED1- | P | Negative backlight voltage |
| **3** | LED2- | P | Negative backlight voltage |
| **4** | NC | | Keep floating |
| **5** | LED+ | P | Positive backlight voltage |
| **6** | NTC | | LED Driver for NTC Function, If not use please keep floating or connect to ground. |
| **7** | VDD | P | Digital power(3.3V) |
| **8** | VDD | P | Digital power(3.3V) |
| **9** | NC | | Keep floating |
| **10** | GND | P | Ground |
| **11** | GND | P | Ground |
| **12** | LV0N | I | LVDS data 0- |
| **13** | LV0P | I | LVDS data 0+ |
| **14** | GND | P | Ground |
| **15** | LV1N | I | LVDS data 1- |
| **16** | LV1P | I | LVDS data 1+ |
| **17** | GND | P | Ground |
| **18** | LV2N | I | LVDS data 2- |
| **19** | LV2P | I | LVDS data 2+ |
| **20** | GND | P | Ground |
| **21** | LVCLKN | I | LVDS CLK- |
| **22** | LVCLKP | I | LVDS CLK+ |
| **23** | GND | P | Ground |
| **24** | LV3N | I | LVDS data 3- |
| **25** | LV3P | I | LVDS data 3+ |
| **26** | GND | P | Ground |
| **27** | SHLR | I | Horizontal scan direction(Normal pull high) |
| **28** | RESET | I | Global reset pin |
| **29** | STBYB | I | Standby mode |
| **30** | UPDN | I | Vertical scan direction(Normal pull high) |
| **31** | GND | P | Ground |

| | | | |
|---|---|---|---|
| **32** | NC | | Keep floating |
| **33** | GND | P | Ground |
| **34** | NC | | Keep floating |
| **35** | GND | P | Ground |
| **36** | VDD | P | Digital power(3.3V) |
| **37** | NC | | Keep floating |
| **38** | VDDA | P | VDDA(13.3V) |
| **39** | VDDA | P | VDDA(13.3V) |
| **40** | NC | | Keep floating |
| **41** | NC | | Keep floating |
| **42** | NC | | Keep floating |
| **43** | VGH | P | VGH( 26V) |
| **44** | NC | | Keep floating |
| **45** | VGL | P | VGL(-7.0V) |
| **46** | NC | | Keep floating |
| **47** | VDD | P | Digital power(3.3V) |
| **48** | VDD | P | Digital power(3.3V) |
| **49** | NC | | Keep floating |
| **50** | GND | P | Ground |

| **SHLR** | **UPDN** | **Data shifting** |
|---|---|---|
| VDD | VDD | Left→Right，UP→Down(default) |
| VDD | GND | Left→Right，Down→UP |
| GND | VDD | Right→Left，UP→Down |
| GND | GND | Right→Left，Down→UP |

**Refer to the figure as below:**



# 3. Electrical Specifications

## 3.1 Absolute Maximum Rating

(GND=0V, Note 3-1)

| Item | Symbol | Values | | Unit | Remark |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Power Voltage | VDD | -0.3 | 4.5 | V | Note 3-1 |
| Power Voltage | VDDA | -0.3 | 14.25 | V | Note 3-1 |
| Power Voltage | VGH | -0.3 | VGL+40 | V | Note 3-1 |
| Power Voltage | VGL | -20 | +0.3 | V | Note 3-1 |
| Operation Temperature | $T_{OP}$ | Ta = -30 | Tp = 85 | ℃ | Note 3-1,2 |
| Storage Temperature | $T_{ST}$ | Ta = -40 | Ta = 90 | ℃ | Note 3-1,2 |
| LED Reverse Voltage | VR | - | 1.2 | V | Each LED |
| LED Forward Current | IF | - | 150 | mA | Each LED |

**Note 3-1 : The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme case, the module may be permanently destroyed.**

**Note 3-2 : Ta = Ambient Temperature, Tp = Panel Surface Temperature.**

### 3.1.1 Typical Operation Conditions

…… Ta=25℃、(GND =0V)

| item | Symbol | Min. | Typ. | Max. | Unit. | Note. |
|---|---|---|---|---|---|---|
| **Digital Supply Voltage** | VDD | 3 | 3.3 | 3.6 | V | Note 3-3、Note 3-4 |
| **Analog Supply Voltage** | VDDA | 13.2 | 13.3 | 13.5 | V | Note 3-3、Note 3-5 |
| **Gate On Voltage** | VGH | 25.5 | 26 | 26.5 | V | Note 3-3 |
| **Gate Off Voltage** | VGL | -7.5 | -7 | -6.5 | V | Note 3-3 |
| **Logic Input Voltage** | VIH | 0.7VDD | - | VDD | V | Note 3-6 |
| | VIL | GND | - | 0.3VDD | V | |

**Note 3-3: VDD、VDDA、VGH、VGL setting should match the signals output voltage of customer's system board.**

**Note 3-4: The ripple voltage should be controlled under 5%.**

**Note 3-5: The ripple voltage should be controlled under 1%.**

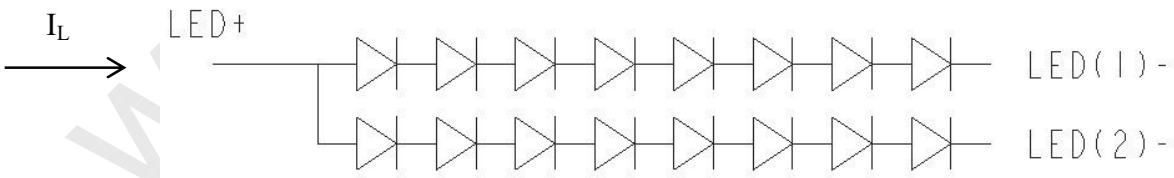
**Note 3-6: SHLR, RESET, STBYB, UPDN.**

### 3.1.2 Backlight Driving Conditions

| Item | Symbol | Values | | | Unit | Remark |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| **Voltage for LED Backlight** | VL | 22.4 | 24.8 | 26.4 | V | Note 3-7 |
| **Current for LED Backlight** | $I_L$ | | 130 | | mA | (2P8S) |
| **LED Life Time** | - | 20000 | | | Hr | Note 3-8 |

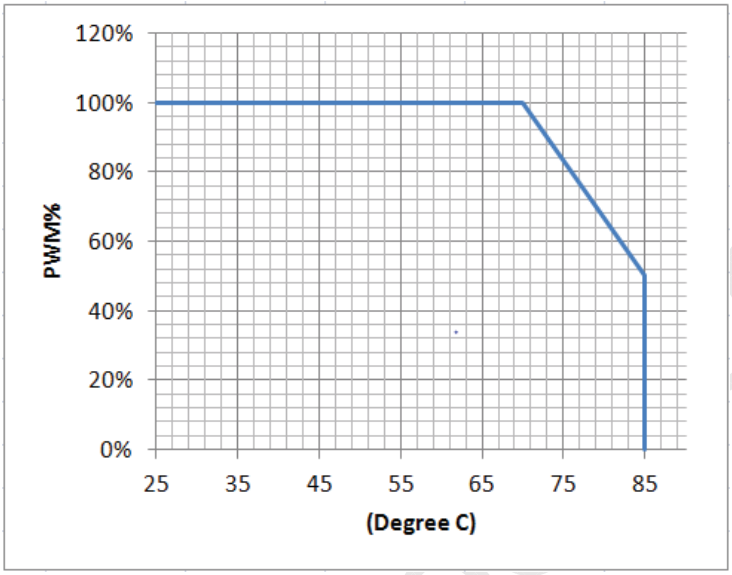
**Note 3-7: The LED Supply Voltage is defined by the number of LED at Ta=25℃ and $I_F$ =150mA.**

**Note 3-8: The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and $I_L$ = 130mA. The LED lifetime could be decreased if operating $I_L$ is lager than 130mA.**



### 3.1.3 PWM.

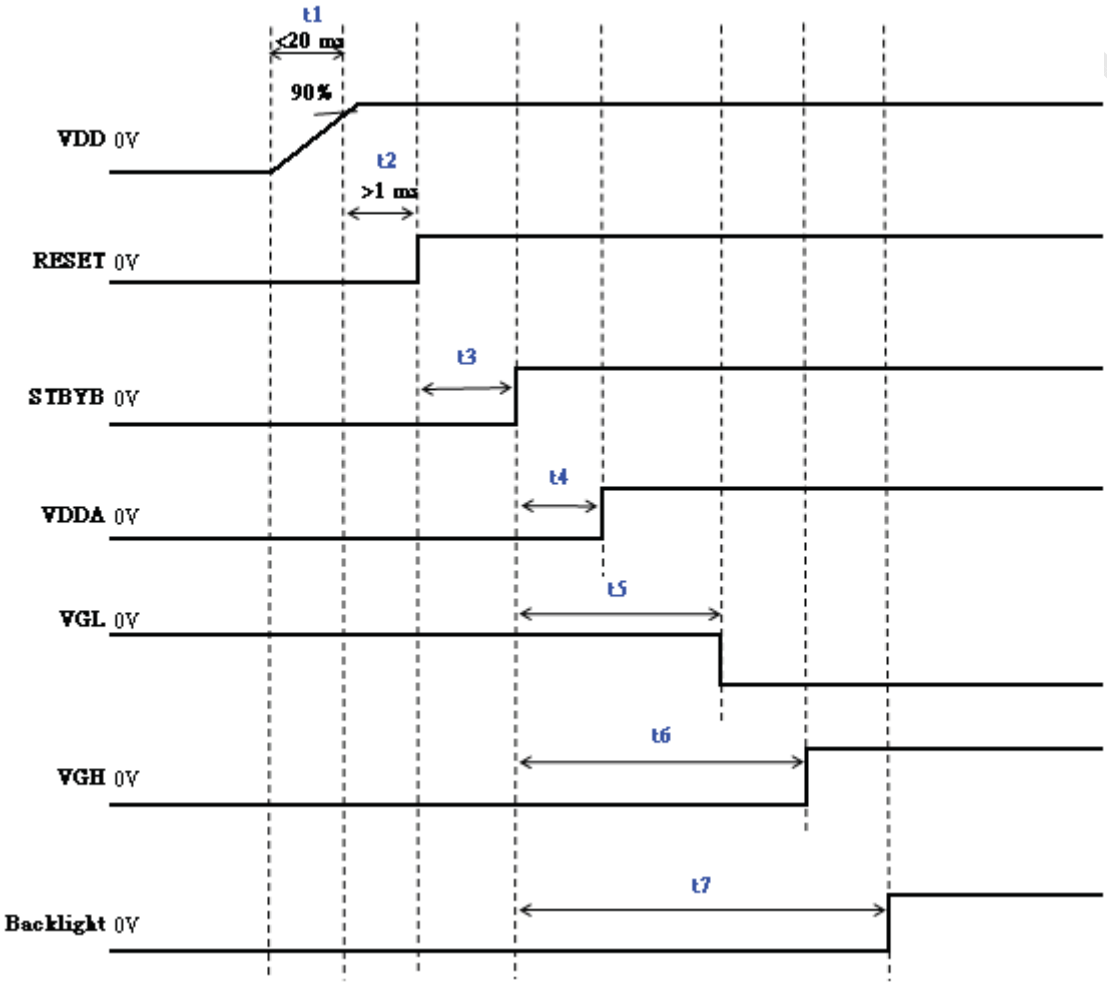
The LED string has a NTC(Negative Temperature Coefficient ) to detect the ambient temperature of LED string.
LED power de-rating has to start at 70℃ linear dow n to PWM 50% at 85℃ before switching off, see graph as below.



## 3.2 Power Sequence

The recommended power on sequence should be: Digital power(VDD) → RESET → STBYB → VDDA → VGL → VGH → Backlight .To power off sequence should be: Backlight → STBYB → VGL & VGH → VDDA → VDD & RESET.

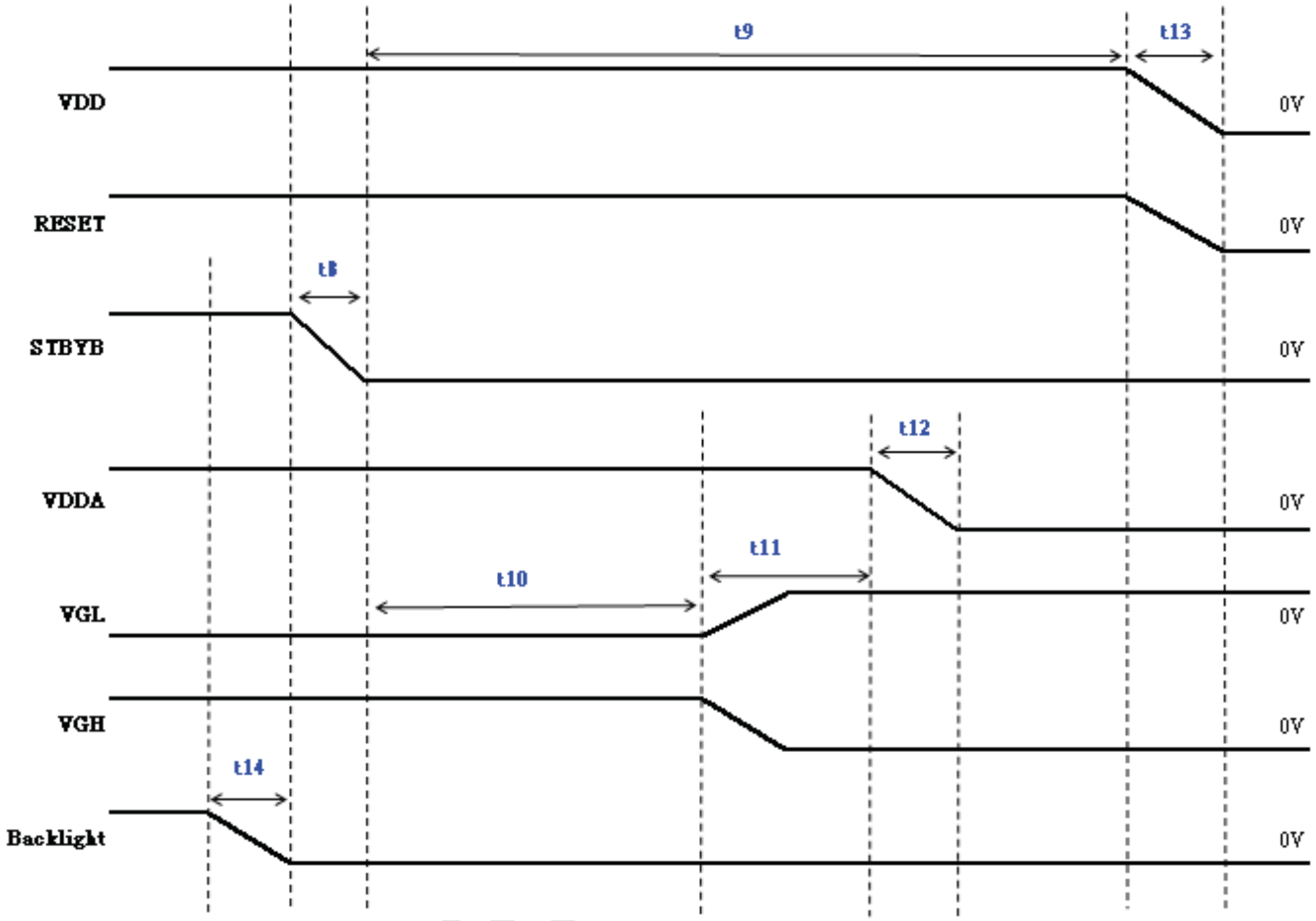
**Power on sequence:**




| Symbol | SPEC. | | | Unit |
|---|---|---|---|---|
| | Min. | Typ. | Max. | |
| t1 | 0 | 5 | 20 | ms |
| t2 | 2 | 3 | 5 | ms |
| t3 | 0 | 5 | 10 | ms |
| t4 | 2 | 3 | 4 | frame |
| t5 | 4 | 5 | 6 | frame |
| t6 | 5 | 6 | 7 | frame |
| t7 | 10 | 11 | 12 | frame |

(1frame = 60Hz)

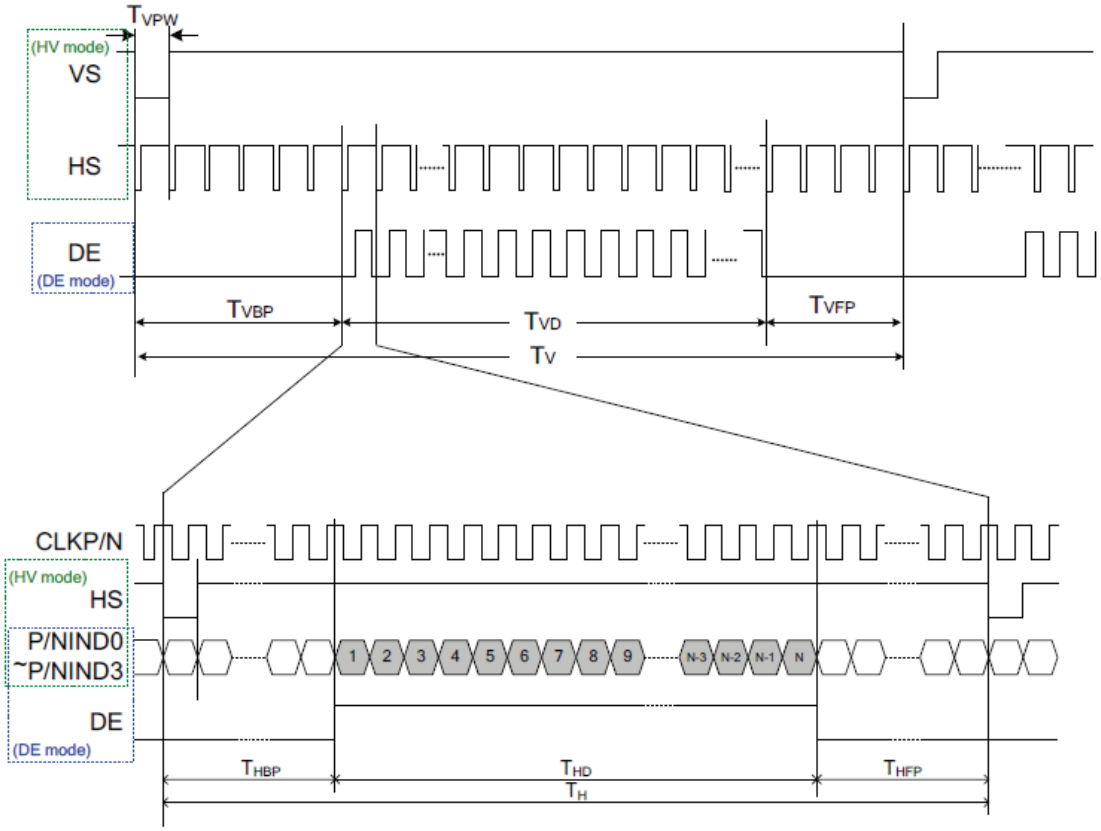
**Power off sequence:**




| Symbol | SPEC. | | | Unit |
|---|---|---|---|---|
| | Min. | Typ. | Max. | |
| t8 | 0 | 2 | 5 | ms |
| t9 | 9 | 10 | 11 | frame |
| t10 | 6 | 7 | 8 | frame |
| t11 | 1 | 2 | 3 | frame |
| t12 | 0 | 2 | 5 | ms |
| t13 | 0 | 2 | 5 | ms |
| t14 | 0 | 10 | 20 | ms |

(1frame = 60Hz)

## 3.3 LVDS Input Timing




Note:
$T_V=T_{VBP}+T_{VD}+T_{VFP}$
$T_H=T_{HBP}+T_{HD}+T_{HFP}$

**Figure. LVDS Input Timing**

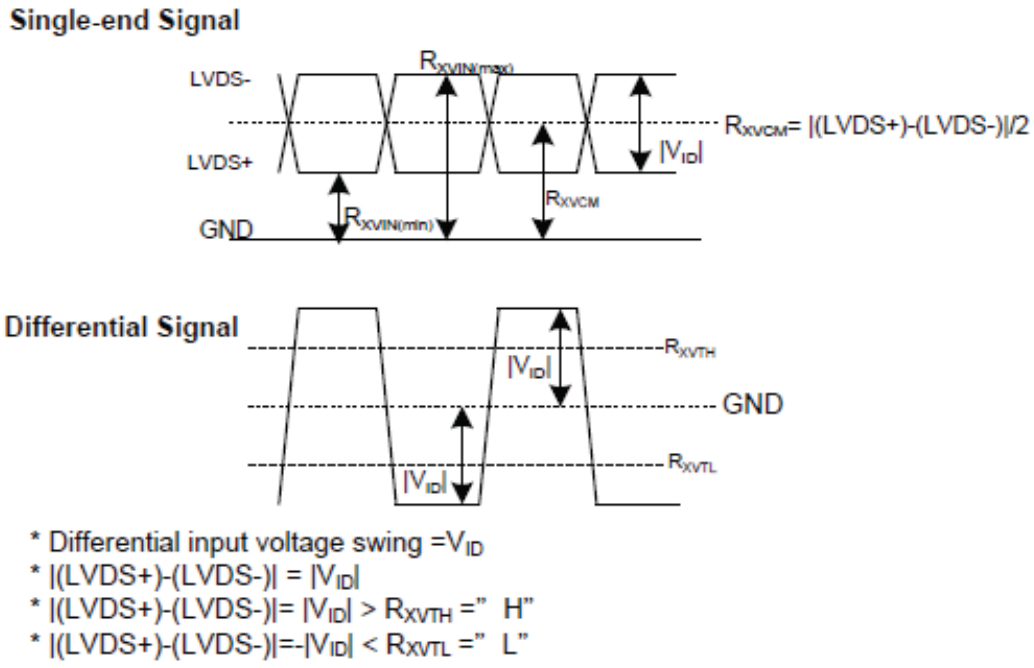
**DE mode for 800x480**

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| CLK frequency | $F_{CLK}$ | 25.2 | 25.4 | 35.7 | MHz |
| Horizontal display area | $T_{HD}$ | | 800 | | CLK |
| HS period time | $T_H$ | 860 | 864 | 974 | CLK |
| HS blanking | $T_{HFP} + T_{HBP}$ | 60 | 64 | 174 | CLK |
| Vertical display area | $T_{VD}$ | | 480 | | H |
| VS period time | $T_V$ | 488 | 490 | 611 | H |
| VS blanking | $T_{VBP} + T_{VFP}$ | 8 | 10 | 131 | H |

### 3.3.1 LVDS DC Interface Electrical Characteristics

(VDD_IF=VDD= 2.7V to 3.6V, VDDA= 8V to 13.5V, GND_IF=GND=GNDA= 0V, $T_J$ = -40°C to +105°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Differential input high threshold voltage | $R_{XVTH}$ | +0.1 | - | - | V | $R_{XVCM}$ =1.2V |
| Differential input low threshold voltage | $R_{XVTL}$ | - | - | -0.1 | V | |
| Input voltage range (singled-end) | $R_{XVIN}$ | 0.7 | - | 1.7 | V | |
| Differential input common Mode voltage | $R_{XVCM}$ | 1 | 1.2 | 1.4 | V | |
| Differential input voltage | $\|V_{ID}\|$ | 0.2 | - | 0.6 | V | |
| Terminal resistor | $R_{TERM}$ | 250 | 300 | 350 | Ω | $T_J$ =+25℃, RTERM[2:0]=HHH |
| Differential input leakage current | $I_{LLVDS}$ | -10 | - | +10 | uA | $T_J$ =+25℃, VDD_IF=3.3V, CLKP/N, DxP/N |
| LVDS Digital Stand-by Current | $I_{STLVDS}$ | - | - | 100 | uA | $T_J$ =+25℃, VDD_IF=3.3V, Input Pin $V_{IH}$=3.3V, $V_{IL}$=0V, Clock & all functions are stopped, STBYB = L |
| LVDS Digital Operating Current | $I_{VDDLVDS}$ | - | - | 60 | mA | $T_J$ =+25℃, VDD_IF=3.3V, Input Pin $V_{IH}$=3.3V, $V_{IL}$=0V, $F_{CLK}$ =85MHz, Input pattern: 55h->AAh->55h->AAh |




* Differential input voltage swing =$V_{ID}$
* |(LVDS+)-(LVDS-)| = $|V_{ID}|$
* |(LVDS+)-(LVDS-)|= $|V_{ID}|$ > $R_{XVTH}$ =" H"
* |(LVDS+)-(LVDS-)|=-$|V_{ID}|$ < $R_{XVTL}$ =" L"

**Figure. LVDS DC Diagram**

### 3.3.2 LVDS Interface AC Electrical Characteristic

(VDD_IF=VDD= 2.7V to 3.6V, VDDA= 8V to 13.5V, GND_IF=GND=GNDA= 0V, $T_J$= -40°C to +105°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Clock frequency | $F_{LVCLK}$ | 20 | - | 85 | MHz | Refer to input timing table for each display resolution. |
| Clock Period | $T_{LVCLK}$ | 50 | - | 11.76 | nsec | |
| Clock high time | $T_{LVCH}$ | - | 4/(7* $R_{XFCLK}$) | - | ns | |
| Clock low time | $T_{LVCL}$ | - | 3/(7* $R_{XFCLK}$) | - | ns | |
| Input data skew margin | $T_{RSKM}$ | - | - | 0.2 | UI | $\|V_{ID}\|$ = 200mV, $R_{XVCM}$ = 1.2V $F_{LVCLK}$ = 85MHz |
| Strobe width | $T_{SW}$ | 0.6 | - | - | UI | |
| 1 data bit time | UI | - | 1/7 | - | $T_{LVCLK}$ | |
| Position 1 | $T_{POS1}$ | -0.2 | 0 | 0.2 | UI | |
| Position 0 | $T_{POS0}$ | 0.8 | 1 | 1.2 | UI | |
| Position 6 | $T_{POS6}$ | 1.8 | 2 | 2.2 | UI | |
| Position 5 | $T_{POS5}$ | 2.8 | 3 | 3.2 | UI | |
| Position 4 | $T_{POS4}$ | 3.8 | 4 | 4.2 | UI | |
| Position 3 | $T_{POS3}$ | 4.8 | 5 | 5.2 | UI | |
| Position 2 | $T_{POS2}$ | 5.8 | 6 | 6.2 | UI | |
| PLL wake-up time | $T_{enPLL}$ | - | - | 150 | us | |
| SSC Modulation Frequency | $SSC_{MF}$ | 23 | - | 93 | KHz | |
| SSC Modulation Rate | $SSC_{MR}$ | -3 | - | +3 | % | $F_{LVCLK}$ =81MHz, Center spread |

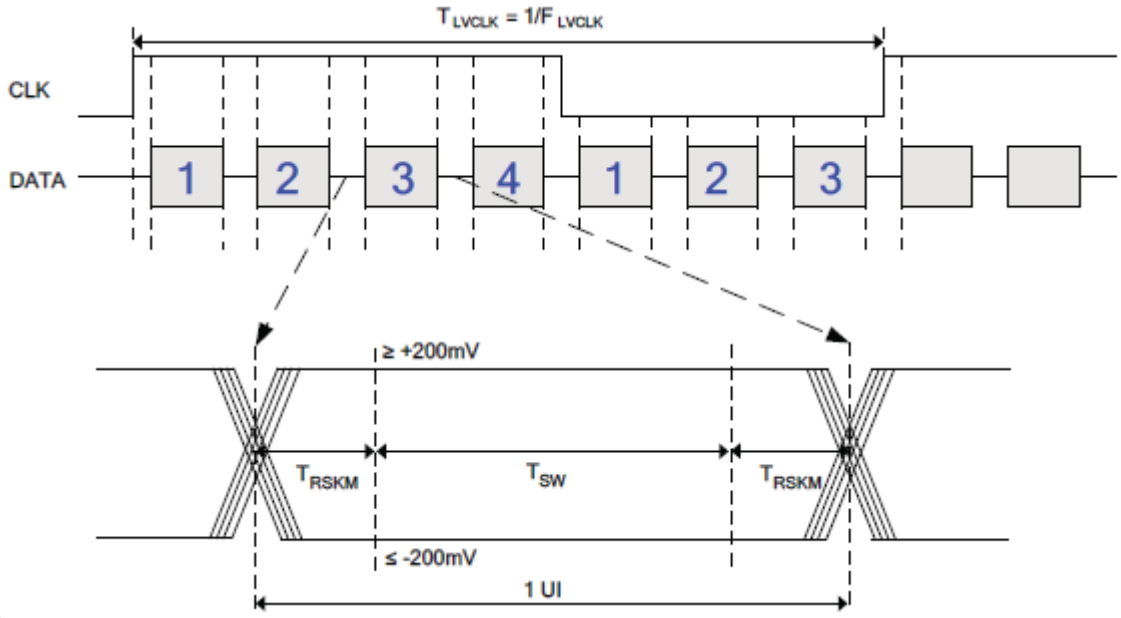



**Figure. LVDS Data Skew**

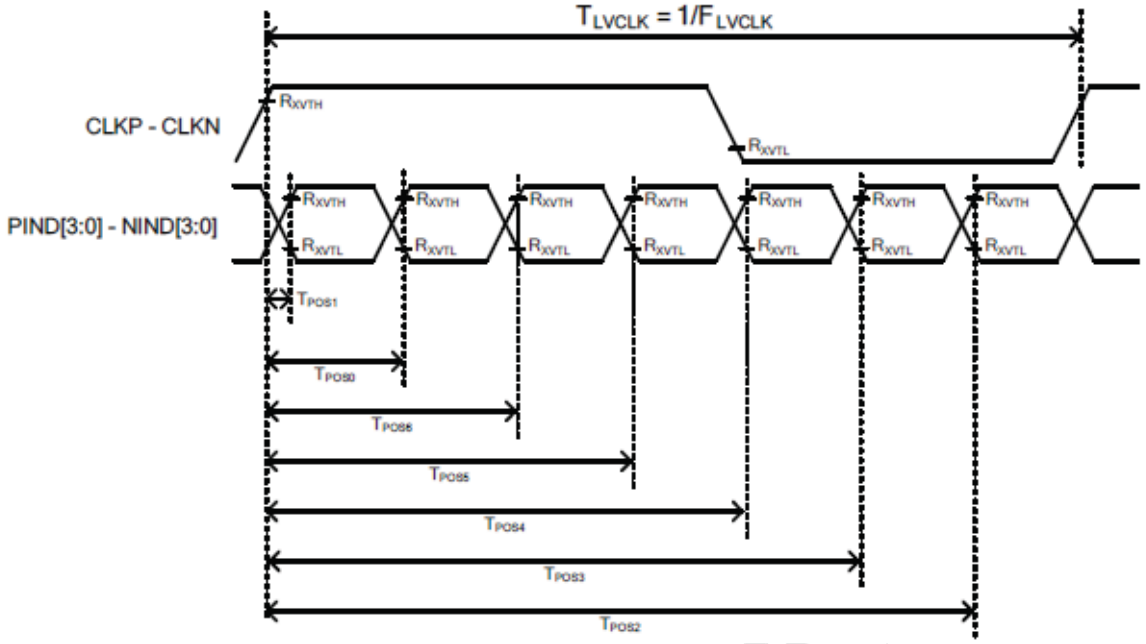



**Figure. LVDS input timing**

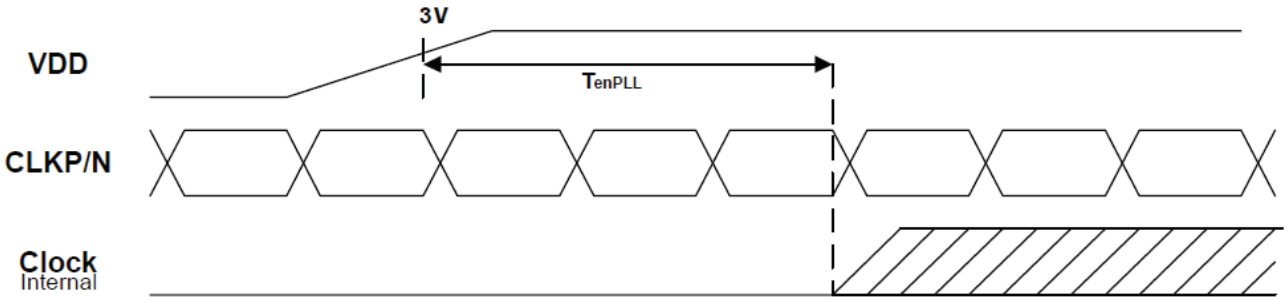



**Figure. Relationship between VDD, LVDS clock, and internal clock**

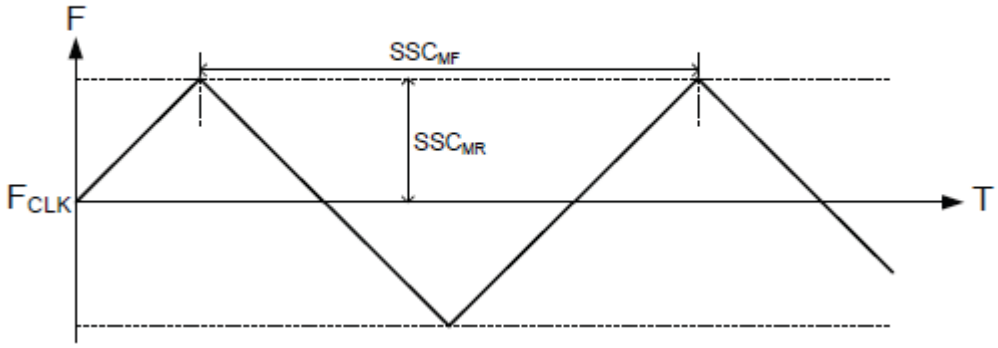



**Figure. Frequency Modulation**

### 3.3.3 Data Input Format for LVDS

**LVDS, 8-bit, JEIDA format**

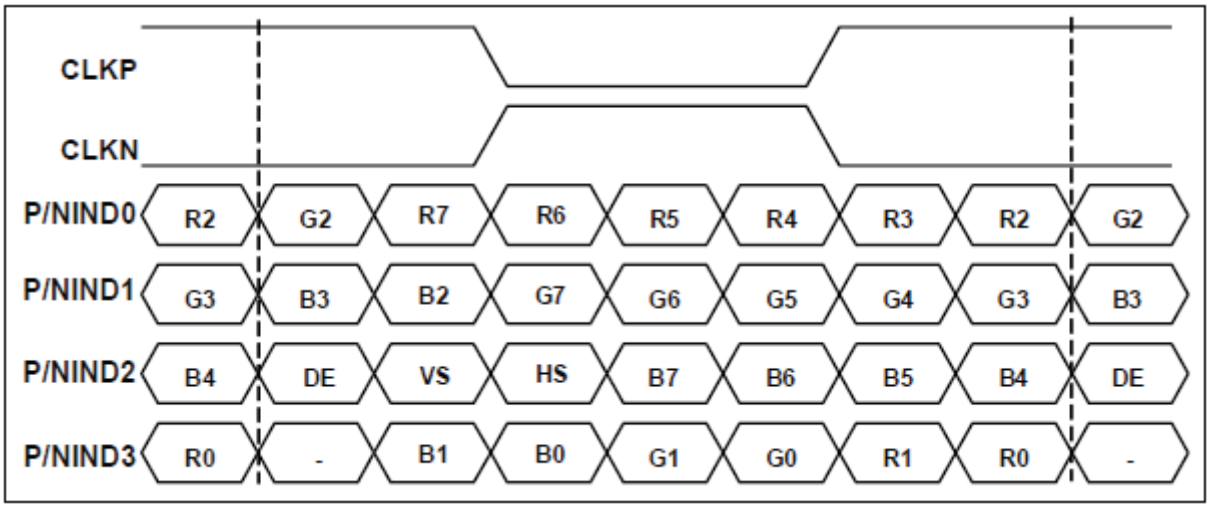



**Figure. 8-bit LVDS Input(JEIDA format)**

### 3.3.4 Reset timing

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| VDD power source slew time | $T_{POR}$ | - | - | 20 | ms | From 0V to 90% VDD |
| GRB active pulse width | $T_{GRB}$ | 1 | - | - | ms | VDD = 3.3V |
| Power on reset voltage | $V_{POR}$ | 0 | - | 100 | mV | |

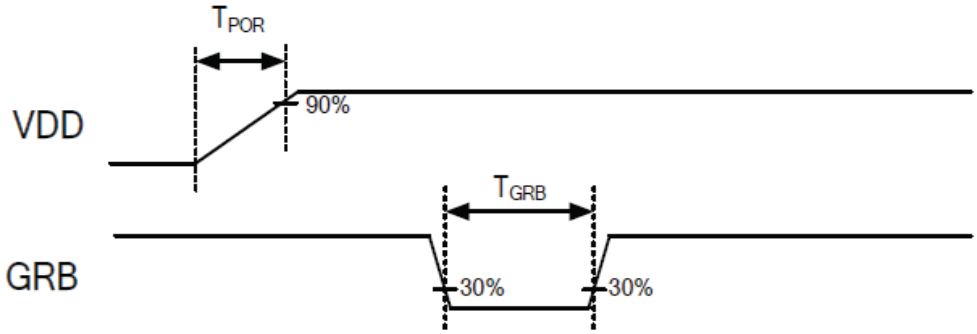



**Figure. Basic AC Timing Chart**

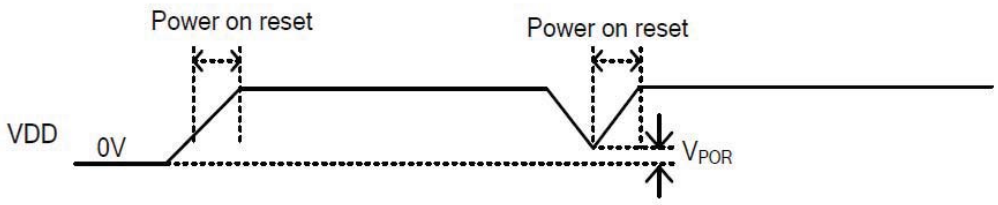



**Figure. Power On Reset Chart**

# 4. Optical Specifications

| Item | Symbol | Condition | Values | | | Unit | Remark |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Viewing Angle (CR≥10) | $\theta_L$ | Φ=180°(9 o'clock) | 70 | 80 | - | degree | Note 4-1 |
| | $\theta_R$ | Φ=0°(3 o'clock) | 70 | 80 | - | | |
| | $\theta_T$ | Φ=90°(12 o'clock) | 70 | 80 | - | | |
| | $\theta_B$ | Φ=270°(6 o'clock) | 70 | 80 | - | | |
| Response Time | $T_{ON}$ | Normal θ=Φ=0° | - | 15 | 20 | msec | Note 4-3 |
| | $T_{OFF}$ | | - | 10 | 15 | msec | |
| Contrast Ratio | CR | | 800 | 1000 | - | - | Note 4-4 |
| Flicker | | | - | - | -20 | dB | Note 4-7 |
| Color Chromaticity | $W_X$ | | 0.270 | 0.310 | 0.350 | - | Note 4-2 Note 4-5 |
| | $W_Y$ | | 0.290 | 0.330 | 0.370 | - | |
| NTSC(CIE 1931) | | | 60 | 70 | - | % | Note 4-2 Note 4-5 |
| Gamma | γ | | 1.9 | 2.2 | 2.5 | | Note 4-2 |
| Luminance (Center) | L | | 600 | 750 | - | cd/m² | Note 4-2 Note 4-5 |
| Luminance Uniformity | YU | | 70 | - | - | % | Note 4-2 Note 4-6 |

**Test Conditions:**

1. **VDD=3.3V, VDDA=13.3V, VGH=26V, VGL=-7.0V, $I_L$= 130mA (Backlight current), the ambient temperature is 25℃**
2. **The test systems refer to Note 4-2.**

**Note 4-1: Definition of viewing angle range**

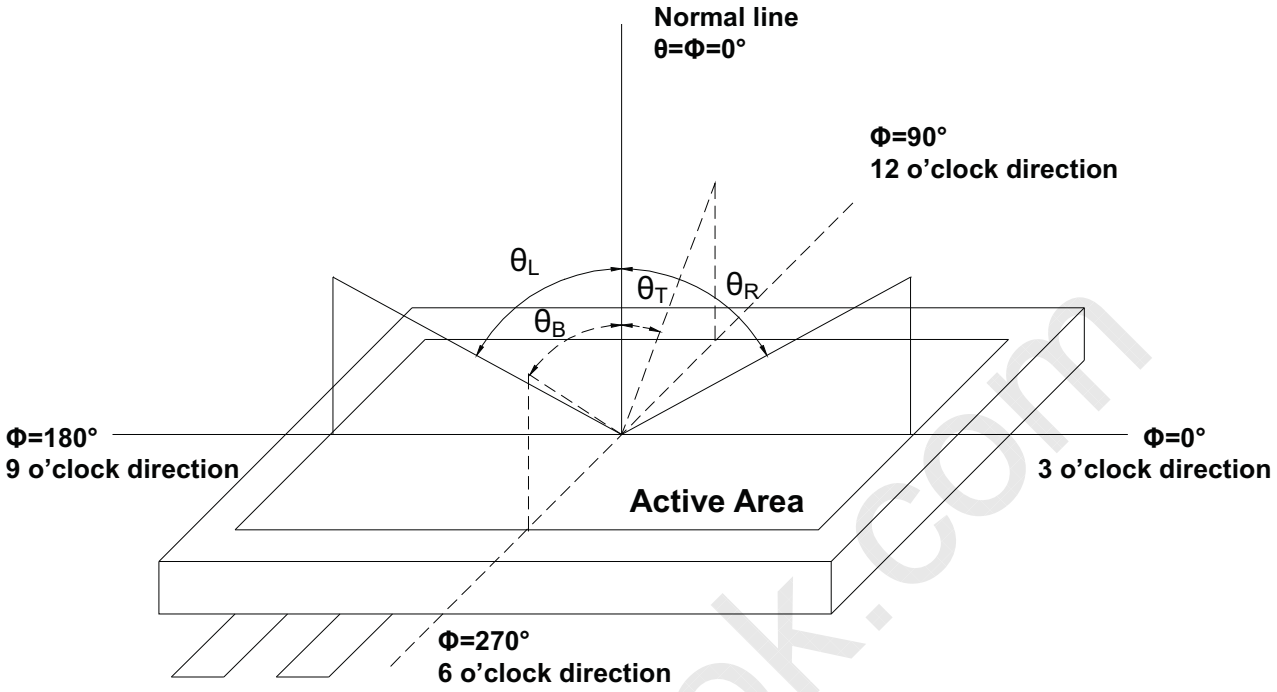



**Fig. 4-1 Definition of viewing angle**

**Note 4-2: Definition of optical measurement system.**
**The backlight has been light on for 10 minutes then measured the optical properties at the center point of the LCD screen in dark room.**

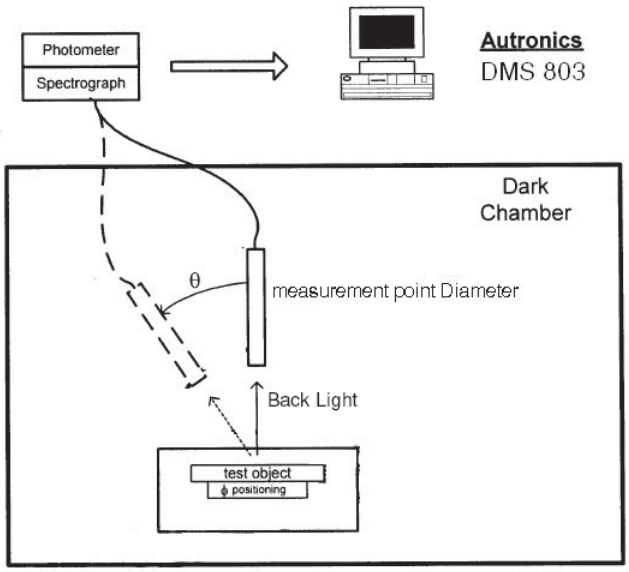



**Fig. 4-2 Optical measurement system setup**

**Note 4-3: Definition of Response time**

**The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (TON) is the time between photo detector output intensity changed from 10% to 90%. And fall time (TOFF) is the time between photo detector output intensity changed from 90% to 10%.**

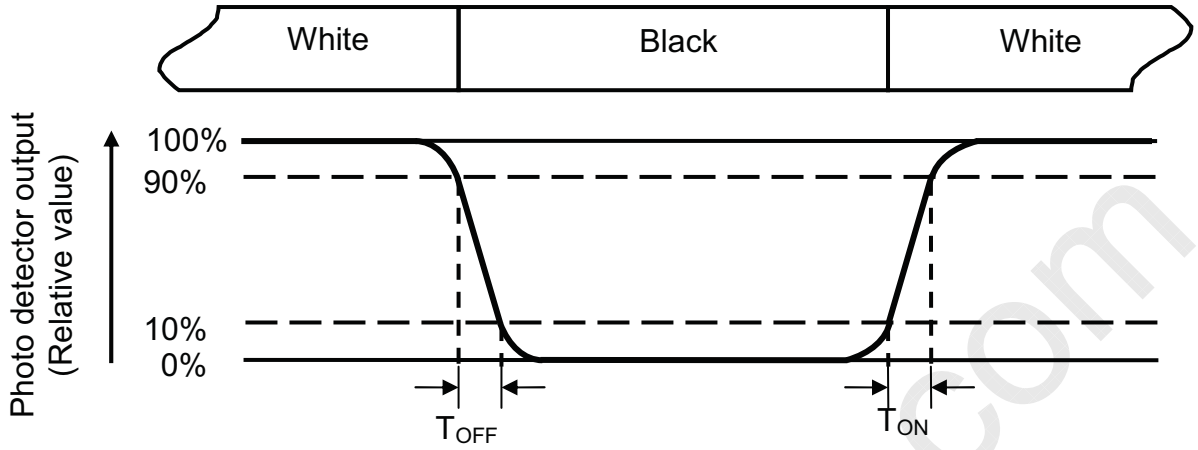



**Fig. 4-3 Definition of response time**

**Note 4-4: Definition of contrast ratio**

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

**Note 4-5: All input terminals LCD panel must be ground while measuring the center area of the panel. The LED BLU driving condition is $I_L$= 130 mA.**

**Note 4-6: Definition of Luminance Uniformity**

**Active area is divided into 9 measuring areas (Refer to Fig. 4-4). Every measuring point is placed at the center of each measuring area.**

$$Luminance\ \ Uniformity\ (Yu) = \frac{B_{min}}{B_{max}}$$

**L-------Active area length W----- Active area width**

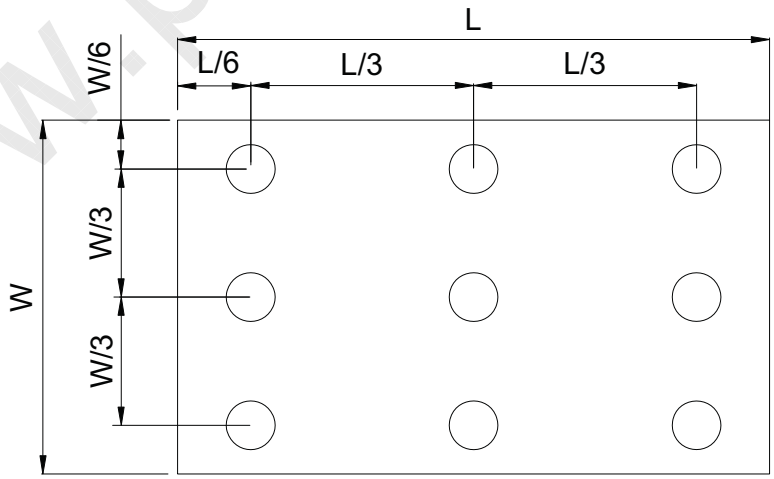



**Fig. 4-4 Definition of measuring points**

**$B_{max}$: The measured maximum luminance of all measurement position.**
**$B_{min}$: The measured minimum luminance of all measurement position.**

**Note 4-7: Definition of flicker.**

**The flicker is measured by JEITA method after module turn-on 120 seconds, under grayscale 128 flicker pattern (Fig. 4-5) at the center point of the LCD screen by CA-210. The luminance signal is processed by FFT analyzer (Fast Fourier Transform Analyzer), and is displayed in a form of energy distribution of frequency components (Fig. 4-6). As shown in Fig. 4-6, when two or more frequency components (P0, Px1, Px2) exist, the maximum value among all the frequency components (Px1, Px2 in the case of Fig. 4-6) except for P0, that is the component of frequency 0, will be set as Px.**

$$\text{Flicker Amount} = 10 \times \log\left(\frac{P_x}{P_0}\right) \text{ [dB]}$$

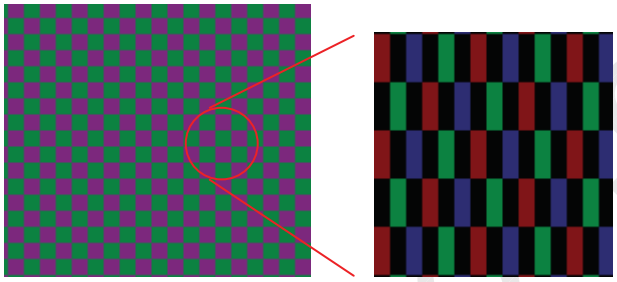


**Fig. 4-5 Flicker pattern of dot inversion**

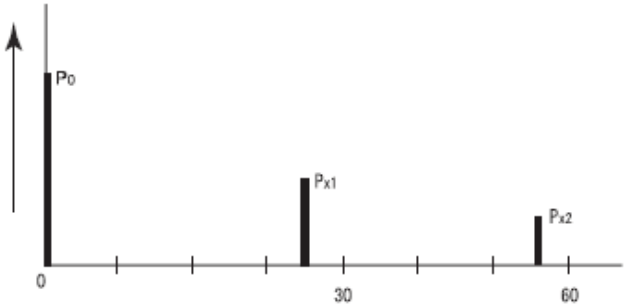



**Fig. 4-6 Energy distribution of frequency components by FFT**

# 5. Reliability Test Items

| Item | Test Conditions | Remark |
|---|---|---|
| High Temperature Storage Test | Ta=90ºC, 500 hours | Note 5-1<br>Note 5-2<br>Note 5-4<br><br>Ta:<br>Ambient<br>Temperature<br><br>Tp:<br>Panel Surface<br>Temperature |
| Low Temperature Storage Test | Ta=-40ºC, 500 hours | |
| High Temperature Operation Test | Tp=85ºC, 500 hours | |
| Low Temperature Operation Test | Ta=-30ºC, 500 hours | |
| High Temperature & High Humidity Operation Test | Ta=60ºC, RH 90%, 500hours | |
| Thermal Shock | (-40℃ 30min)→(85℃ 30min)]/cycle，100 cycles | |
| ESD Test | Condition 1 : C = 150pF, R = 330Ω Contact Discharge, ± 8KV<br>Condition 2 : C = 150pF, R = 330Ω, Air Discharge, ± 15KV | Note 5-1 |
| Mechanical Shock | 100G, 6ms, half sine wave, 3 times for each direction of ±X, ±Y, ±Z | Note 5-1<br>Note 5-3 |
| Mechanical Vibration | Duration: 8 hrs (X-Axis), 8 hrs (Y-Axis), 8 hrs<br>(Z-Axis)<br>Effective Acceleration = 19.6 m/s2 = 2.0 GRMS | Note 5-1<br>Note 5-3 |
| Packaging Vibration Test | 1.14Grms<br>[spectrum：1Hz,4Hz,100Hz, 200Hz]<br>Bottom : 30min/Axis<br>Right-Left & Front-Back : 15min/Axis. | |
| Packaging Drop Test | 1corner, 3edges, 6faces (1 time/direction)<br><follow ISTA(1A) height><br>0kg≦W <10kg：76cm,<br>10kg≦W <19kg：61cm,<br>19kg≦W <28kg：46cm,<br>28kg≦W <45kg：31cm,<br>45kg≦W ≦68kg：20cm | |

**Note 5-1 criteria : Normal display image with no obvious non-uniformity and no line defect.**

**Note 5-2 Evaluation should be tested after storage at room temperature for more than two hour**

**Note 5-3 At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.**

**Note 5-4 A certain level of Mura (non-uniformity) of dark / black image will happen several days after high temperature testing (H.T.T.). There is a slowly part recovery over a long time (several months).Such a long exposure time like in H.T.T. will normally not happen in a real application. Therefore the test H.T.T. was introduced to simulate cycles with normal conditions in-between but with the same total exposure time what show a significant reduced Mura. The root cause is related to tension generated due to different amount of shrinking in the stack of layers in the polarizer sheet. The effect is more significant on larger displays like this size. An investigation into alternative polarizer material showed that there is no better alternative currently available.**

# 6. General Precautions

## 6.1 Safety

**Liquid crystal is poisonous. Do not put it in your mouth. If liquid crystal touches your skin or clothes, wash it off immediately by using soap and water.**

## 6.2 Handling

1. The LCD panel is plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.

2. The polarizer attached to the display is easily damaged. Please handle it carefully to avoid scratch or other damages.

3. To avoid contamination on the display surface, do not touch the module surface with bare hands.

4. Keep a space so that the LCD panels do not touch other components.

5. Put cover board such as acrylic board on the surface of LCD panel to protect panel from damages.

6. Transparent electrodes may be disconnected if you use the LCD panel under environmental conditions where the condensation of dew occurs.

7. Do not leave module in direct sunlight to avoid malfunction of the ICs.

## 6.3 Static Electricity

1. Be sure to ground module before turning on power or operating module.

2. Do not apply voltage which exceeds the absolute maximum rating value.

## 6.4 Storage

1. Store the module in a dark room where must keep at 25±10℃ and 65%RH or less.

2. Do not store the module in surroundings containing organic solvent or corrosive gas.

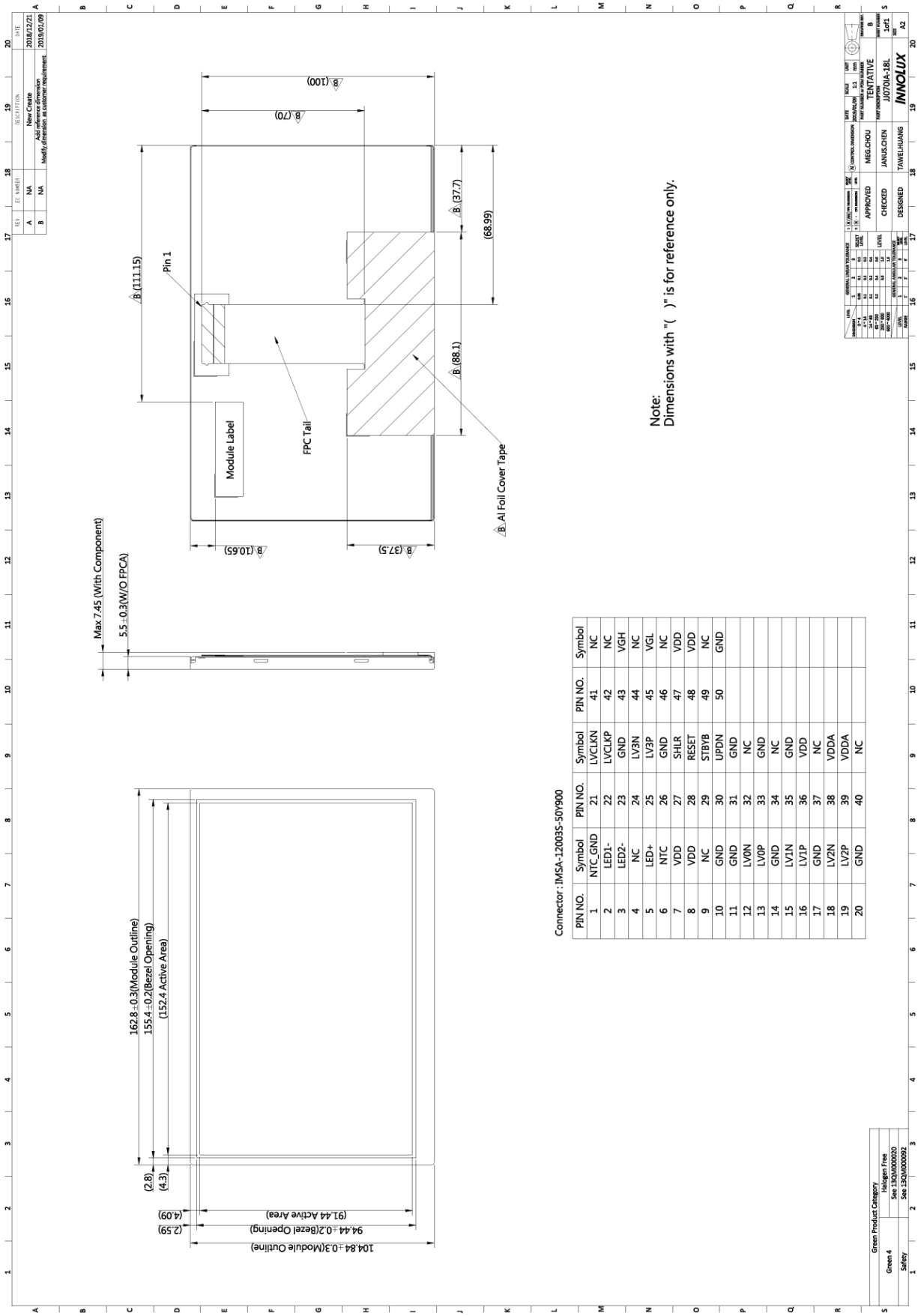
3. Store the module in an anti-electrostatic container or bag.

## 6.5 Cleaning

1. Do not wipe the polarizer with dry cloth. It might cause scratch.

2. Only use a soft sloth with IPA to wipe the polarizer, other chemicals might permanent damage to the polarizer.

# 7. Mechanical Drawing




| PIN NO. | Symbol | PIN NO. | Symbol | PIN NO. | Symbol |
|---|---|---|---|---|---|
| 1 | NTC_GND | 21 | LVCLKN | 41 | NC |
| 2 | LED1- | 22 | LVCLKP | 42 | NC |
| 3 | LED2- | 23 | GND | 43 | VGH |
| 4 | NC | 24 | LV3N | 44 | NC |
| 5 | LED+ | 25 | LV3P | 45 | VGL |
| 6 | NTC | 26 | GND | 46 | NC |
| 7 | VDD | 27 | SHLR | 47 | VDD |
| 8 | VDD | 28 | RESET | 48 | VDD |
| 9 | NC | 29 | STBYB | 49 | NC |
| 10 | GND | 30 | UPDN | 50 | GND |
| 11 | GND | 31 | GND | | |
| 12 | LV0N | 32 | NC | | |
| 13 | LV0P | 33 | GND | | |
| 14 | GND | 34 | NC | | |
| 15 | LV1N | 35 | GND | | |
| 16 | LV1P | 36 | VDD | | |
| 17 | GND | 37 | NC | | |
| 18 | LV2N | 38 | VDDA | | |
| 19 | LV2P | 39 | VDDA | | |
| 20 | GND | 40 | NC | | |

# 8. Packing Drawing